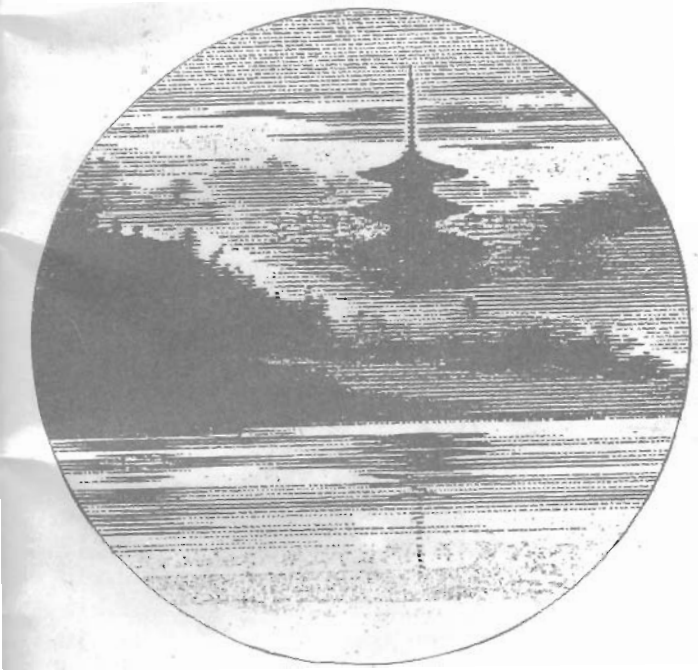
# ISCAS '85

## 1985 INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS



June 5—7, 1985

Kyoto Hotel

Kyoto, Japan

## ADVANCE PROGRAM


CAS

THE INSTITUTE OF ELECTRONICS AND COMMUNICATION ENGINEERS OF JAPAN

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

**S7AI** **Friday, June 7**
**Room I 1:30 pm to 5:00 pm**

Special Session

## Systems Approach for Power Systems Engineering

***Organizer/Chairman:*** F.F. Wu, *University of California, Berkeley, CA, USA*
***Organizer:*** H. Haneda, *Kobe University, Kobe, Japan*
***Co-Chairman:*** T. Sakaguchi, *Mitsubishi Electric Corporation, Amagasaki, Japan*

**S7AI. 1: Transient Stability Analysis of Power Systems with Transmission Losses**
Y. Ohta, M. Sasaki, Tadashi Matsumoto, *Fukui University, Fukui, Japan*

**S7AI. 2: An Intelligent Support System for Power System Planning**
R. Fujiwara, T. Sakaguchi, Y. Kohno, Hiroshi Suzuki, *Mitsubishi Electric Corporation, Amagasaki, Japan*

**S7AI. 3: Geometric Approach to Bad Data Analysis in Electric Power System State Estimation**
R.J. Kaye, *University of New South Wales, Australia*

**S7AI. 4: Performance Indices for Measuring the Robustness of Power System Operation**
R. Fischl, F. Merced, *Drexel University, Philadelphia, PA, USA*

**S7AI. 5: Analysis of Vulnerability of Power Network Configurations**
C.C. Liu, *University of Washington, Seattle, WA, USA*
F.F. Wu, *University of California, Berkeley, CA, USA*

**R7EA** **Friday, June 7**
**Room A 6:30 pm to 9:00 pm**

Regular Session

## VLSI Design Architecture

***Chairman:*** G.D. Hachtel, *University of Colorado, Boulder, CO, USA*
***Co-Chairman:*** T. Chiba, *Sharp Corporation, Tenri, Japan*

**R7EA. 1: A Data-Flow Array Convolver for Two-Dimensional Convolution**
K. Onaga, *Hiroshima University, Higashi-Hiroshima, Japan*, H. Kawanishi, *NEC Corporation, Nakahara, Kawasaki, Japan*

**R7EA. 2: Design and VLSI Implementation of a Concurrent Solver for N Coupled Least-Squares Fitting Problems**
E.F. Deprettere, K. Jainandunsing, *Delft University of Technology, Delft, Netherlands*

**R7EA. 3L: A New Technique for Symbolic Function Generation Using Number Theoretic Transform**
W.C. Siu, *Hong Kong Polytechnic, Hong Kong*, Chih-Fan Chen, *Chinese University of Hong Kong, Hong Kong*

**R7EA. 4: A VLSI Implementation of RNS-Based Architectures**
M.A. Bayoumi, G.A. Jullien, W.C. Miller, *University of Windsor, Windsor, ONT, Canada*

**R7EA. 5L: A Low Cost Design Environment for Custom and Semi-Custom Integrated Circuit Design**
A. Legrand, G.K. Egan, I. Donaldson, *Royal Melbourne Inst. of Technology, Melbourne, Australia*

**R7EA. 6: A Functional Operation Architecture for Image Processing**
L. Palmier, *ETCA/CTME/OP, Arcueil Cedex, France*, F. Devos, *I.E.F., Orsay Cedex, France*, C. Legrand, *ETCA/CTME/OP, Arcueil Cedex, France*, B. Zavidovique, *AFDAC/ETCA, Paris, France*

**R7EA. 7L: On the Architecture of a Monolithic Median Filter with Variable Window Widths**
N. Kanopoulos, J.J. Hallenbeck, *Research Triangle Institute, Research Triangle Park, NC, USA*

**R7EB** **Friday, June 7**
**Room B 6:30 pm to 9:00 pm**

Regular Session

## Design and Testing of Logic Circuits

***Chairman:*** H. Fujiwara, *Meiji University, Tokyo, Japan*

**R7EB. 1: Fault Identification in t-Diagnosable Systems for Fault Tolerant Computation**
F. Lombardi, *University of Colorado, Boulder, CO, USA*

**R7EB. 2: PROD: A VLSI Fault Diagnosis System**
P. Odryna, A. Strojwas, *Carnegie-Mellon University, Pittsburgh, PA, USA*

**R7EB. 3: New Directions in the Design for Testability in VLSI Circuits**
I.L. Sayers, G. Russell, D.J. Kinniment, *University of Newcastle Upon Tyne, Newcastle Upon Tyne, UK*