JOINT ROYAL MELBOURNE INSTITUTE OF TECHNOLOGY AND
COMMONWEALTH SCIENTIFIC AND INDUSTRIAL RESEARCH ORGANISATION
PARALLEL SYSTEMS ARCHITECTURE PROJECT

Directory of Parallel Computing Research Projects in Australia

TR 118 085 R

D. Abramson †

† Division of Information Technology
C.S.I.R.O.
§ c/o Department of Communication and Electronic Engineering
Royal Melbourne Institute of Technology
P.O. Box 2476V
Melbourne 3001
Australia.

Version 1.0 June 1989

ABSTRACT:

Parallel computing is an emerging technology in which there are many unresolved research issues. This document consists of a collection of project descriptions of research being conducted into parallel programming within Australian research institutes. The aim of the report is to try and increase the sharing of information about this research, with particular attention to the Australian research environment.

Introduction

Parallel computing is an emerging technology in which there are many unresolved research issues. This document consists of a collection of project descriptions of research being conducted into parallel programming within Australian research institutes. The aim of the report is to try and increase the sharing of information about this research, with particular attention to the Australian research environment.

The importance of parallel computing is being recognised by special research centres being established. A collaborative venture between CSIRO and RMIT in Melbourne has been running since 1986. This joint project has specific goals, such as the development of parallel computer systems and languages, as well as the general goal of transferring parallel computing technology into the Australian industry. The centre has a number of experimental and commercial parallel processors. ANU in Canberra has also established a special parallel computing initiative, and has acquired parallel computing equipment. No doubt, other such centres will be created over the next few years.

Much of the information in this report was gathered from the Australian computer network news, and thus may not include projects for sites which do not have access to ACSNET. Investigators for research projects which are not in the current release should contact the editor so that their project descriptions can be included in the next release. Further, as projects are created and completed the chief investigators should send in new entries to the editor.

Thanks go to those who took the time and effort to respond to the survey request, and even more so to those who collected and co-ordinated the responses from their own sites.

This work was performed under the CSIRO/RMIT Parallel Systems Architecture Project, which is a collaborative project being jointly supported by CSIRO Division of Information Technology, and the Royal Melbourne Institute of Technology.

Dr David Abramson
Senior Research Scientist
Division of Information Technology
C.S.I.R.O.
c/o Department of Communication and Electrical Engineering
RMIT,
124 LaTrobe St,
Melbourne, 3000.
E-mail rcoda@koel.co.rmit.oz

Title of Project: The MultiView Distributed Integrated Programming Environment

Chief Investigators: Dr. C. D. Marlin

Institution: The University of Adelaide

Starting date and duration: Started Jan. 1985 (ongoing)

Funding Sources: ARGS/ARC, ACRB/ATERB, University. of Adelaide, Sun Microsystems, Apple Computer

Number of People on Project (Full Time/Fractional): 3/9
(incl. postgraduate students, Hons. students, academic staff)
(1 full-time at U. of A., 2 full-time at DSTO,
8 fractional at U. of A., 2 fractional at DSTO)

Hardware Developed: N/A

Software Developed: Prototype of the MultiView environment; at this stage, permits editing, but not execution.

Abstract: (25 lines or less)

Since early 1985, the MultiView Project within the Centre for Computer Systems and Software Engineering has been investigating a particular approach to the construction of integrated programming environments: the provision of multiple concurrent views of the program under construction.

The user of the system has the ability to simultaneously display a number of views of the program being developed. This ability improves programmer productivity by allowing different parts of the program to be viewed in different ways, and at different levels of detail, depending on the needs of the programmer at the time.

The implementation of the MultiView programming environment is a distributed system, consisting of a collection of parallel processes communicating via message-passing. At present, this distributed program runs on a network of Sun workstations and servers, and will eventually be also ported to the Leopard multiprocessor workstation, also being developed at the University of Adelaide.

Publications List:

R. A. Altmann, "An Abstract Syntax Tree Editor for the MultiView Programming Environment", Honours project report, Department of Computer Science, The University of Adelaide, Adelaide, South Australia (October 1986).

R. A. Altmann, A. N. Hawke and C. D. Marlin, "An Integrated Programming Environment Based on Multiple Concurrent Views", Australian Computer J., Vol. 20, No. 2 (May 1988), pp.65--72.

R. A. Altmann, A. N. Hawke and C. D. Marlin, "MultiView: An Integrated Incremental Programming Environment with Multiple Concurrent Views", Proc. Seminar on Parallel Computing Architectures, Telecom Research Laboratories, Clayton, Victoria, February 1986), pp.171--180.

Contact : Dr. C.D. Marlin E-mail: marlin@cs.ua.oz.au
Department of Computer Science
The University of Adelaide
G.P.O. Box 498
Adelaide, S.A. 5001
Australia

Title of Project: A Study of Parallel Processing Architectures for Simulating and proving Integrated Circuits at the Design Stage.

Chief Investigators: Bruce Tonkin (PhD student)

Institution: University of Adelaide

Starting date and duration: 1987-90

Funding Sources: ATERB Postgraduate Scholarship, Commonwealth Postgraduate Scholarship, AT&T Bell Laboratories.

Number of People on Project (Full Time/Fractional): 1

Hardware Developed: No direct parallel hardware has been developed.

Software Developed: Developed software on experimental MIMD parallel machine at AT&T Bell Laboratories, U.S.A to perform circuit extraction in parallel.

Abstract: (25 lines or less)

A VLSI circuit must be thoroughly verified before it is submitted for fabrication. As designs get larger the time taken to verify the circuit increases exponentially. A key element of this process is circuit extraction in which the geometric layout used for fabrication is analyzed to obtain accurate circuit parameters. Current work has focussed on techniques that allow large circuits to be analyzed with limited primary memory resources available on a small scale parallel processor. Efficient access to secondary storage is currently been researched.

Publications List: Work currently submitted for publication.

Contact: Bruce Tonkin E-mail: btonkin@augean.oz
Department of Electrical and Electronic Engineering
University of Adelaide.

Title of Project: The Leopard Multiprocessor Project

Chief Investigators: Prof. Chris J. Barter, Mr. Peter J. Ashenden

Institution: University of Adelaide

Starting data and duration: 1985--90

Funding Sources ARC, CSIRO, DSTO

Number of People on Project (Full Time/Fractional): 5/5

Hardware Developed: Leopard-1 Multiprocessor (completed 1987), Leopard-2 Multiprocessor (under design)

Software Developed: -

Abstract: (25 lines or less)

The Leopard Multiprocessor Project group is designing and developing a high performance symmetric multiprocessor. Prototyping has been completed with the 3-processor Leopard-1, which includes a graphics capability.

A major research goal is to investigate the role of cache memories and associated cache coherence strategies in multiprocessor machines.

Design work on the Leopard-2, which uses National Semiconductor NS32532 processors, is in the final stages. Testing of fabricated boards is expected to begin during September/October 1989, with a complete operational system available in February 1990.

After completion of the base Leopard-2, research will continue into cache coherence strategies using the Leopard-2 and purpose built cache controllers which can be plugged in and programmed.

Publications List:

Please write or e-mail to contact person for current publication list.

Contact: Peter J. Ashenden E-mail: petera@cs.ua.oz.au
Department of Computer Science
GPO Box 498, Adelaide, SA 5001, Australia
Phone: +61 8 228 5198

Title of Project: Software Development in a Data Flow Environment

Chief Investigators: Dr. Andrew L Wendelborn

Institution: University of Adelaide

Starting date and duration: April 1988

Funding Sources: CSIRO

Number of People on Project (Full Time/Fractional): 1

Hardware Developed: N/A

Software Developed: SISAL compiler in SISAL; performance evaluation suite

Abstract: (25 lines or less)

The primary aim of the project is to use the programming language SISAL to construct a compiler for a realistic subset of SISAL. In general terms, the main areas of interest are:

to provide a non-numeric application program for the RMIT data flow machine

to investigate concurrency in the compilation process itself, especially in lexical analysis and parsing, but also between phases of the compilation process and with multiprogrammed compilations

to suggest a methodology for compiler construction in a parallel environment

to investigate the suitability of SISAL's stream interface for modular program construction, and for expressing program input/output

Publications List:

Wendelborn, A.L., Garsden, H.B., Irlam, G., McDonald, I.D., Smith, G.M. "The Development and Efficient Execution of SISAL Programs", Proceedings of "Dataflow: A status Report", Prentice-Hall, in print.

Contact: Dr. Andrew L Wendelborn
Dept. of Computer Science,
University of Adelaide
GPO Box 498
Adelaide 5001

E-mail: andrew@chook.ua.oz

Title of Project: Run-Time Systems for Multiprocessor Execution of Functional Programs

Chief Investigators: Dr. Andrew L Wendelborn

Institution: University of Adelaide

Starting date and duration: June 1988

Funding Sources: University of Adelaide Research Grant

Number of People on Project (Full Time/Fractional): 1

Hardware Developed: N/A

Software Developed: SISAL support software on Encore Multimax under Mach

Abstract: (25 lines or less)

The aim of this research is to investigate suitable run-time models for the execution of functional language programs on multi-processor architectures. This complements existing Departmental projects for the construction of a multiprocessor system (the Leopard project), and compiler development in the functional programming language SISAL. It also investigates methods for the effective use of recently acquired Departmental hardware and software, specifically, Encore Multimax computers and the Mach operating system.

To this end, the project has three principal objectives:

to develop SISAL applications on the Encore multiprocessor, and evaluate their performance

to express an existing run-time model in terms of Mach operating system primitives, and investigate the facilities offered by Mach for relatively fine-grained tasking

to examine the implications for a microtasking run-time system of a multiprocessor architecture with some local memory, such as the Leopard-2, and design a run-time system architecture suitable for the Leopard-2

Publications List: in preparation

Contact: Dr. Andrew L Wendelborn
Dept. of Computer Science,
University of Adelaide
GPO Box 498
Adelaide 5001

E-mail andrew@chook.ua.oz

Title of Project: Familiarization with parallel computing using Transputers

Chief Investigators: Russell Creek, Angela Melkis, Dr Tim Monks, Dr Ralph MacNally, Craig Blundell

Institution: BHP - Melbourne Research Laboratories

Starting date and duration: Project not yet started and is presently open-ended

Funding Sources: BHP Corporate funding for new technology of relevance to the core businesses.

Number of People on Project: 1-3 part time

Hardware developed: N/A

Software developed: N/A

Abstract:

As most image processing and data analysis tasks encountered by our group require much computation and since this computation needs to be performed rapidly, parallel computing techniques are being investigated. Transputers offer an economical and powerful introduction to parallel computing and so a Definicom board is being purchased and will be used to gain familiarity with programming using the message passing paradigm.

Publications List: none in this area

Contact Person: Russell Creek E-mail: russell@merlin.bhpmrl.oz
Image Processing and Data Analysis Group,
BHP Melbourne Research Labs,
245 Wellington Rd, Mulgrave, Vic.
(03) 566 7439

Title of Project: Neural Accelerator Board (NAB)

Chief Investigators: Dr. Charles Watson,

Institution: Defence Science and Technology Organisation,

Starting date and duration: 1988 - 1991

Funding Sources: Defence Dept.

Number of People on Project (Full Time/Fractional): 3

Hardware Developed: prototype arithmetic chips

Software Developed: Simulators

Abstract: (25 lines or less)

The NAB is a co-processor board for SUN workstations, implemented as an array of ASIC processors. It calculates pipe-lined sums of products at the rate of 30,000,000,000 operations per second (30 GOPS) and will be used as a high-speed classifier. The first prototype concept demonstrator is planned for November 1989.

The initial design is a VME board with 64 custom VLSI chips, each containing 16 8-bit processors. On-chip memory can be loaded from the VME interface, and fed in parallel to the processors. The architecture is systolic with both data and microcode flowing through the array, and can be SIMD with shared microcode or MIMD with independent microcode. The system is time multiplexed by a factor of 16 to match the chip processing power with chip bandwidth.

The immediate application areas for the concept demonstrator include:

RADAR Signature Recognition
Real-time video multi-spectral classification
Real-time video processing of 16 sets of 16 by 16 convolution masks
Synthetic Aperture Radar (SAR) Imaging and Pattern Recognition
Sonar classification
Speaker Independent Speech Recognition

Publications List:

"The Computer Analysis of Polyphonic Music", Proc. 22nd ANZAAS Conference, Brisbane, May 1981.

"Algorithms for the separation of Superimposed Tones", Proc. 1st Conference on Music and Technology, Melbourne, August 1981.

"SPRINT Functional Specification", Internal working document, VLSI-IWD-82-12-1, CSIRO. (co-author)

AUSMPC Project Report, May 1982, CSIRO VLSI Program.

"A Floorplan Algebra and Composition Paradigm for VLSI Design", Technical Report, VLSI-TR-83-3-1, CSIRO.

"A Proposal for a Silicon Implementation Language (SIL)", Technical Report, VLSI-TR-83-3-2, CSIRO.

"An Algorithm for the Correct Interconnection of VLSI-Level Macrocells", Proc. VLSI Pacific Asian Region Conference, Melbourne, May 1984.

"A Declarative Design Approach for Combining Macrocells by Directed Placement and Constructive Routing", Proc. 21st Design Automation Conference, New Mexico, June 1984. (co-author)

"Speaker-Dependent Word Recognition - A Case Study of a Custom VLSI Chip Development", Proc. IEEE International Conference on Computer Design: VLSI in Computers, New York, Oct 1984. (co-author)

"The Computer Analysis of Polyphonic Music", Ph.D. Thesis, University of Sydney, 1985.

"An Algorithm for the Correct Interconnection of VLSI-Level Macrocells", Journ.Electrical and Electronics Engineering, Australia. Sept 1985.

"The Design of a Parallel LISP/Prolog Machine", Internal Working Document, Div. Information Technology, CSIRO, 1986.

"VLSI Design", First ASEAN Science and Technology Conference, Kuala Lumpar, April 1986. (co-author)

"A Custom IC Design for a Multi-Memory Mapping Unit", Proc. Aust. Microelectronics Conference, Adelaide, May 1986.

"Automated Layout of CMOS Circuits", Proc. Aust. Microelectronics Conference, Melbourne, April 1987.

"A Tool Set for Correct-by-Construction VLSI Design", Proc. Electronic Design Automation Conference, Wembley, England, July 1987. (co-author)

"A CAD System for the Rapid Design of Custom Integrated Circuits", Proc. NELCON, Auckland, New Zealand, September 1987.

"A Rapid Design System for Custom Integrated Circuits", Digest of papers IREECON, Sydney, September 1987.

"An Hierarchical Index for Relational Databases", (to be published)

"A Neural Network Architecture", Proc. Aust. Symposium on Signal Processing and Applications, Adelaide, April 1989.

Contact : Dr. Charles Watson, E-mail: crw@itd.dsto.oz
Information Technology Div,
ERL, DSTO,
PO Box 1600,
Salisbury, SA 5108
(08) 259 6128

Title of Project: The Design and Implementation of Parallelism in Systems and Applications for Shared Memory Multi-Processor Machines

Chief Investigators: Rhys Francis

Institution: La Trobe University

Starting date and duration:

Multiprocessor Simulator	1985 - ongoing
MultiThreaded Programming	1989 - 1991

Funding Sources:

1989	$42,798 ARC	MultiThreaded Programming
	$5,000 SIGMA	Postgraduate Bursary (A.N.Pears)
1988	$5,000 LTU	Synchronous Execution on Multiprocessors
	$5,000 SIGMA	Postgraduate Bursary (A.N.Pears)
	$2,500 SIGMA	Postgraduate Bursary (I.D.Mathieson)
	$3,000 LMI	Access to a Sequent at Sigma Data in Sydney
1987	$7,900 LTU	Threads: MIMD machine Programming
	$5,000 SIGMA	Postgraduate Bursary (I.D.Mathieson)
	$3,194 LMI	Mixed Stack Architectures
1986	$4,043 LTU	MIMD machine modeling
	$1,000 LMI	MIMD machine modeling
1985	$1,990 LMI	International Conference Attendance
	$1,700 LMI	Compiler Development

ARC = Australian Research Council, LTU = La Trobe University Research Committee, LMI = School of Mathematical and Information Sciences Research Committee, SIGMA = Sigma Data Corporation.

Number of People on Project (Full Time/Fractional): 2 / 4 (current, varies from year to year)

Hardware Developed: N/A

Software Developed: A Multiprocessor Simulator and Embedding Compiler Parallel Kernel and Applications

Abstract: (25 lines or less)

This project aims to derive algorithms and demonstrate corresponding implementations which exhibit 'best possible' speedup on multi-processor systems. It also aims to find effective expressions and realizations for the invocation, cessation and synchronization of parallel execution in systems and applications.

The Threads project aims to develop programming models which support realizable parallel speedup and effective mappings onto shared memory multiprocessor architectures. It is based on the concept of multiple simultaneous execution points within a single program executing in a shared process context. The project encompasses language features for expressing parallelism, implementation strategies for locating, scheduling and synchronizing parallel execution, and architectural enhancements to the multiprocessor machine class.

Publications List:

PAPERS

R.S. Francis and L.J.H. Pannan,"Parallelism in QuickSort", Proc. 12th Aust. Comp. Sci. Conf., February 1989, pp. 353--361.

R.S. Francis and A.N. Pears,"An Error Recovery Tool for Yacc",Proc. 12th Aust. Comp. Sci. Conf., February 1989, pp. 65--74.

R.S. Francis and I.D. Mathieson, "A Benchmark Parallel Sort for Shared Memory Multiprocessors",IEEE Transactions on Computers, Vol. 37, No. 12, December 1988, pp. 1619--1626.

R.S. Francis and I.D. Mathieson, "Synchronised Execution on Shared Memory Multi-Processors",Journal of Parallel Computing, Vol. 8, 1988, pp. 165--175.

I.D. Mathieson and R.S. Francis, "A Dynamic-Trace-Driven Simulator for Evaluating Parallelism", Proc. 1988 Hawaii Int. Conf. on System Sciences, Vol I, Hawaii, January 1988, pp. 158--166.

R.S. Francis and I.D. Mathieson, "Parallel Procedure Calls", Proc. 1987 IEEE Int. Conf. on Parallel Processing, Chicago, August 1987, pp. 663--666.

R.S. Francis and I.D. Mathieson, "A Threaded Programming Environment", Aust. Computer Science Communications, Vol. 9, No. 1, February 1987, pp. 173--183.

R.S. Francis, "Ultracomputers: Serialization Free Synchronization" Seminar on Parallel Computing Architectures",Telecom Australia Research Labs., 10 pages, February 1986.

R.S. Francis and I.D. Mathieson, "A Library of Languages for Exploring Concurrency",Proc. 9th Aust. Comp. Sci. Conf., January 1986, pp. 95--105.

I.D. Mathieson and R.S. Francis, "Parallel Procedure Calls", Winter UNIX Conference, Brisbane, 1985.

REPORTS

R.S. Francis and L.J.H. Pannan, "An Examination of Parallel Execution in Quicksort", Technical Report 1/89, Department of Computer Science, La Trobe University, January 1989.

R.S. Francis and A.N. Pears,"Error recovery in a Lex-Yacc parser", Technical Report 11/88, Department of Computer Science, La Trobe University, December 1988.

R.S. Francis and I.D. Mathieson, "A Parallel Merge and Sort", Technical Report 3/88, Department of Computer Science, La Trobe University, May 1988.

I.R. Francis, "Functional Programming Languages, Theory and Implementation" M.Sc. Prelim. thesis, Department of Computer Science, La Trobe University, December 1987.

A. Pears, "The Application of Concurrency in Computer Graphics", Honours thesis, Department of Computer Science, La Trobe University, December 1987.

S. Campbell, "Distributed Systems: Architectures, Languages and Operating systems", Honours thesis, Department of Computer Science, La Trobe University, December 1987.

I.D. Mathieson and R.S. Francis, "An Evaluation of Parallel Procedure Calls", Technical Report 2/87, Department of Computer Science, La Trobe University, June 1987.

G. Seregeg, "Effective Execution of Parallel Algorithms", Honours thesis, Department of Computer Science, La Trobe University, December 1986.

R.S. Francis and I.D. Mathieson, "Threads: Machine Model and Emulation", Technical Report 6/86, Department of Computer Science, La Trobe University, December 1986.

R.S. Francis, "Threads: Language Reference Manual", Technical Report 5/86, Department of Computer Science, La Trobe University, December 1986.

R.S. Francis, "CONC: A parallel programming language", Technical Report 10/85, Department of Computer Science, La Trobe University, December 1985.

Contact: Dr. Rhys Francis E-mail: rhys@latcs1
Department of Computer Science
Bundoora
Victoria, 3083

Title of Project: Parallel Simulation of Analog Networks (suitable for modelling neural networks)

Chief Investigators: David Suter

Institution: La Trobe University

Starting date and duration: June 1989 - 3 years

Funding Sources: La Trobe University ($21500)

Number of People on Project (Full Time/Fractional): 2

Hardware Developed: Recently purchased 8 transputer network

Software Developed: None as yet

Abstract: (25 lines or less)

Our knowledge of vision gained from artificial intelligence and from neuroscience has enabled us to formulate neural network theories of early vision processing.In order to test these theories we need to build models of these networks that can be simulated on computers. We are embarking upon a program of design and simulation of analog neural networks suitable for vision processing (such as stereopsis, shape from shading, motion estimation, edge detection). The simulation and design process is extremely computationally expensive, and thus requires the development of parallel methods for problem solution.

Networks are modelled by a large set of (non-linear) equations, these equations are solved using iterative techniques that are multi-level and multi-rate using the correct level of abstraction and temporal precision for the part of the net under investigation. Such methods ought to allow parallel asynchronous solution.

Publications List:

D. Suter "Analog Signal Processing: Applications in Computer Vision,"to be presented 1989 Aust. Symp. on Signal Processing and Applications,Adelaide, April 1989.

D. Suter and X. Deng. "Simulation of Neural Nets on Transputers," IEEE Systems, Man, and Cybernetics Conference, pp. 694-697, Aug. 1988.

Contact: David Suter
Dept. Computer Science,
La Trobe University,
Bundoora 3083.
E-mail: suter@latcs1.oz

Title of Project: Stereo Vision System

Chief Investigators: David Suter

Institution: La Trobe University

Starting date and duration: April 1989 - 3-5 years

Funding Sources: none as yet

Number of People on Project (Full Time/Fractional): 2

Hardware Developed:

Software Developed: Initial stages of multiresolution edge detection in each visual channel - implemented on an 8 transputer network.

Abstract: (25 lines or less)

The basic theory proposes that a set of features are extracted from each image at different scales of resolution. Then the set of feature maps are matched at each level by using potential matches at other levels to guide matching in a cooperative manner. There are a number of proposals as to how this cooperation is best achieved; furthermore, in some cases, it has been suggested that the efficiency and reliability of the system would be greatly enhanced by extending the cooperative effort to include monocular depth cues such as shape from shading, depth from focus, texture gradient. These proposals are generally not supported by enough detailed experimentation or comparison.

The project is to investigate efficient methods for cooperative solution of the stereopsis problem using a transputer network. This transputer network will enable the implementations to be investigated in an interactive manner.

Publications List:

D. Suter, X. Deng, H. A. Cohen, and T. S. Dillon "Development and Implementation of Parallel Vision Algorithms," to appear Vision'89, Detroit, April 1989.

D. Suter and H. A. Cohen "Incorporating knowledge via regularization theory: applications in vision and in image processing," Proceedings AI'88, Adelaide, pp. 389-404, Nov 1988.

Contact: David Suter
Dept. Computer Science,
La Trobe University,
Bundoora 3083.
E-mail: suter@latcs1.oz

Title: Machine Intelligence Project - Parallel NU-Prolog

Chief Investigators: Lee Naish

Other Investigators: Jeff Schultz

Institution: University of Melbourne

Starting date and duration: 87, ongoing

Funding Sources: ARC, DISC Computers

Number of People on Project (Full Time/Fractional): 2

Hardware Developed: nil

Software Developed: Parallel NU-Prolog (ongoing)

Abstract: (25 lines or less)

NU-Prolog is a dialect of Prolog with primitives to enable coroutining and with improved handling of negation. A deterministic subset of the language can be run using "stream AND-parallelism" (similar to Parlog, Guarded Horn Clauses and Concurrent Prolog), without encountering problems with distributed backtracking. A preprocessor has been implemented which allows code in the deterministic subset of NU-Prolog to be written more easily and the NU-Prolog system has been modified to run this code in parallel. The current (prototype) implementation runs on an Encore (and should be easy to port to other shared memory multiprocessors running Unix).

The second part of the project, just beginning, is to implement an OR-parallel version of NU-Prolog. The implementation will be based on ideas from BC-Prolog (a system running on special purpose hardware), but we will use a shared memory multiprocessor. Eventually we hope to combine the OR-parallel system with the stream AND-parallel system.

Publications List:

Lee Naish: Negation and control in Prolog, Lecture Notes in Computer Science 238, Springer-Verlag, New York, 1986, p. 119.

Lee Naish: Negation and quantifiers in NU-Prolog, Proceedings of the Third International Conference on Logic Programming, London, England, July 1986, pp. 624-634.

James Thom, Justin Zobel (Eds.): NU-Prolog reference manual, version 1.0, Technical Report 86/10, Department of Computer Science, University of Melbourne, Melbourne, Australia, 1986.

Lee Naish: Parallelizing NU-Prolog, Proceedings of the Fifth International Conference/Symposium on Logic Programming, Seattle, Washington, August 1988, pp. 1546-1564.

Lee Naish: Proving properties of committed choice logic programs, Journal of Logic Programming, to appear.

Contact: Lee Naish
Department of Computer Science,
University of Melbourne,
Parkville, 3052 Victoria
E-mail: lee@cs.mu.oz.au

Title: Machine Intelligence Project - Parallel logic programming - Ptah

Chief Investigators: Zoltan Somogyi, Kotagiri Ramamohanarao (Rao)

Other Investigators: Mark Ross (RMIT)

Institution: University of Melbourne

Starting date and duration: 87, ongoing

Funding Sources: ARC, ATERB

Number of People on Project (Full Time/Fractional): 3

Hardware Developed: nil

Software Developed: Ptah (ongoing)

Abstract: (25 lines or less)

The aim of the Ptah project is to build a parallel logic programming system oriented towards large-scale software production and not towards research into AI and databases (the traditional focus of logic programming so far). Unlike Prolog, Ptah relies on extensive compile-time checks. It has a strong type system, which also serves as the basis of a novel system of strong modes that enforces regular and controlled patterns of information flow between program components. Compile-time knowledge of these patterns allows the Ptah execution algorithm to combine stream AND-parallelism with don't-know nondeterminism (in the form of either backtracking or OR-parallelism) in an efficient manner.

Ptah needs this stream AND-parallelism because it is intended to be suitable for system programming on parallel machines (among other things), and stream AND-parallelism is the natural logic programming representation of parallel communicating processes. We are investigating several issues that arise when a language like Ptah is applied to operating system: the main issue we have addressed so far is control of nondeterminism.

We are also exploring new architectures that can run parallel logic programs efficiently. Since we believe that memory latency will be a problem in parallel logic machines, due to the poor locality of logic programs, we have so far concentrated on ways of reducing the effect of long memory latencies. We believe that when running programs written in an inherently parallel language (such as Ptah), simple barrel processors can improve not only system throughput but also the runtime of a single program.

Publications List:

Zoltan Somogyi: A system of precise modes for logic programs, Proceedings of the Fourth International Conference on Logic Programming, Melbourne, Australia, May 1987, pp. 769-787.

Zoltan Somogyi, Kotagiri Ramamohanarao, Jayen Vaghani: A stream AND-parallel execution algorithm with backtracking, Proceedings of the Fifth International Conference/Symposium on Logic Programming, Seattle, Washington, August 1988, pp. 1142-1159.

Zoltan Somogyi, Kotagiri Ramamohanarao, Jayen Vaghani: A backtracking algorithm for the stream AND-parallel execution of logic programs, International Journal of Parallel Programming, to appear.

Zoltan Somogyi: Stability of logic programs: how to connect don't-know nondeterministic logic programs to the outside world, Technical Report 87/11, Department of Computer Science, University of Melbourne, submitted to the Journal of Logic Programming.

Zoltan Somogyi, Mark Ross, Kotagiri Ramamohanarao: Tolerance of latency in parallel logic programming machines, Informal Proceedings of the Workshop on Concurrent Programming, Tokyo, Japan, December 1988.

Zoltan Somogyi: A parallel logic programming system based on strong and precise modes, Technical Report 89/4, Department of Computer Science, University of Melbourne, January 1989, p. 146, Ph.D. thesis.

Contact: Zoltan Somogyi E-mail: zs@cs.mu.oz.au
Department of Computer Science,

University of Melbourne,
Parkville, 3052 Victoria

Title: Machine Intelligence Project - Aditi - a parallel deductive database

Chief Investigators: Kotagiri Ramamohanarao (Rao)

Other Investigators: Jayen Vaghani, John Shepherd, David Kemp, David Keegel

Institution: University of Melbourne

Starting date and duration: 88, ongoing

Funding Sources: ARC, DISC Computers, DITAC

Number of People on Project (Full Time/Fractional): 5

Hardware Developed: nil

Software Developed: Aditi (ongoing)

Abstract: (25 lines or less)

Aditi is a deductive database that is intended to have performance competitive with commercial database products on relational tasks while at the same time supporting new computational paradigms. An Aditi database can contain rules and structured data as well as traditional tuples of atomic items. Relations can use any of a number of file structures, including variable-bucket B-trees, multi-key hashing, superimposed coding and bang files. The work is done by a Query Server that coordinates the work of several RAPs (Relational Algebra Processors). The RAPs can perform the traditional operations union, select, project, and join as well as operations needed for the support of differential bottom-up computation, such as merge-with-difference. The Query Server assigns work to the RAPs on behalf of Database Access Programs that interpret a low-level language; this language is the target for a compiler that accepts NU-Prolog-like programs. This compiler puts source programs through magic set transformations as well as other transformations that push query constraints into the body of the program as far as possible. It then generates code that performs differential bottom-up computation for the transformed program.

Publications List:

Kotagiri Ramamohanarao, John Shepherd, Isaac Balbin, Graeme Port, Lee Naish, James Thom, Justin Zobel, Philip Dart: The NU-Prolog deductive database system, Prolog and databases, Ellis Horwood, Chicester, England, 1988, pp. 212-250.

James A. Thom, Lee Naish, Kotagiri Ramamohanarao: A superjoin algorithm for deductive databases, in Foundations of Deductive Databases and Logic Programming, Morgan Kaufmann Publishers, 1988, pp. 519-544.

I. Balbin, K. Ramamohanarao: A generalization of the differential approach to recursive query evaluation, Journal of Logic Programming, 4:3, September 1987, pp. 259-262.

R. Sacks-Davis, A. Kent, K. Ramamohanarao: Multikey access methods based on superimposed coding techniques, ACM Transactions on Database Systems, 12:4, December 1987, pp. 655-696.

Isaac Balbin, Krishnamurthy Meenakshi, Kotagiri Ramamohanarao: A query independent method for magic set computation on stratified databases, Proceedings of the 1988 International Conference on Fifth Generation Computer Systems, Tokyo, Japan, December 1988, pp. 711-718.

Kotagiri Ramamohanarao, John Shepherd: A superimposed codeword indexing scheme for very large Prolog databases, Proceedings of the Third International Conference on Logic Programming, London, England, July 1986, pp. 569-576.

Lee Naish, James A. Thom, Kotagiri Ramamohanarao: Concurrent database updates in Prolog, Proceedings of the Fourth International Conference on Logic Programming, Melbourne, Australia, May 1987, pp. 178-195.

Kotagiri Ramamohanarao, John A. Shepherd: Answering queries in deductive database systems, Proceedings of the Fourth International Conference on Logic Programming, Melbourne, Australia, May 1987, pp. 1014-1033.

David Kemp, Krishnamurthy Meenakshi, Kotagiri Ramamohanarao, Isaac Balbin: Propagating constraints in recursive deductive databases, Technical Report 89/6, Department of Computer Science, University of Melbourne, 1989.

Contact: Kotagiri Ramamohanarao E-mail: rao@cs.mu.oz.au
Department of Computer Science,
University of Melbourne,
Parkville, 3052 Victoria

Title: Melbourne University optoelectronic multicomputer project

Chief Investigators: A.B. (Tobias) Ruighaver

Institution: University of Melbourne

Starting date and duration: 88, ongoing

Funding Sources: Department of Computer Science, University of Melbourne

Number of People on Project (Full Time/Fractional): 4

Hardware Developed: AMD29000 Processing Element (ongoing)
FDDI back-end network (ongoing)

Software Developed: Parallel Modula-2 (ongoing)

Abstract: (25 lines or less)

The Optoelectronic Multicomputer Project investigates the efficient exploitation of small-to-medium granularity parallelism in scientific applications. To close the gap between current commercial parallel systems and the more general purpose (but still unsuccessful) data flow machines, we are developing advanced semi-dataflow programming techniques and an improved multicomputer architecture with optical communication. Semi-dataflow programming techniques are a promising tool for efficient and portable programming of parallel architectures. The language Parallel Modula-2 (PM2) developed for this project, supports a simple semi-dataflow programming model. Although related to dataflow languages, PM2 offers an easy to use deterministic construct for explicit parallelism and a new abstraction mechanism based on static instantiation of objects. Initially, we will support PM2 on a MacIntosh II with multiple AMD29000 coprocessors. To connect several of these Mac II's in a distributed parallel system we are developing a 100 Mbit/s optical (FDDI) LAN link. FDDI will also provide a back-end network for our proposed large-scale multicomputer architecture. A new optical communication system, with a higher density than hypercube topologies, will remove many of the disadvantages of current static-scheduling multicomputer systems. To implement such dense interconnection networks we will be extending our research in the area of high-speed optoelectronic transducer design.

Publications List:

A.B. Ruighaver: Design aspects of the Delft parallel processor DPP84 and its programming system, SIGARCH Computer Architecture News, 14:1, January 1986, pp. 4-8.

A.B. Ruighaver: Hierarchical programming and the DPP84, Ph.D. thesis, Technical University of Delft, Delft, Netherlands, 1986, p. 115.

E.E.E. Friedman, A.B. Ruighaver: An electro-optical data communication system for the Delft parallel processor, SIGARCH Computer Architecture News, 15:6, December 1987, pp. 2-8.

A.B. Ruighaver: A proposal for the Melbourne University optoelectronic multicomputer project, Technical Report 88/6, Department of Computer Science, University of Melbourne, Melbourne, Australia, March 1988.

A.B. Ruighaver: The Melbourne University Optoelectronic Multicomputer Project, SCS Summer Conference, Seattle, July 1988.

T.T.E. Yeo, A.B. Ruighaver: PM-2: an exercise in deterministic parallel programming, Technical Report 89/3, Department of Computer Science, University of Melbourne, Melbourne, Australia, January 1989.

Contact: A.B. (Tobias) Ruighaver
Department of Computer Science,
University of Melbourne,
Parkville, 3052 Victoria
E-mail: tobias@cs.mu.oz.au

Title of Project: Parallel Reasoning in Recursive Causal Networks

Chief Investigators: W. Wen and E. A. Sonenberg

Institution: University of Melbourne

Starting date and duration: 3/1988, 1 year

Funding Sources: A Commonwealth postgraduate award

Number of People on Project (Full Time/Fractional):1/1

Hardware Developed:

Software Developed: Parallel interpreter of RCNDL (Recursive Causal Network Description Language) for Encore

Abstract: (25 lines or less)

A parallel probabilistic reasoning method in Recursive Causal Networks (RCNet) is proposed based on information theory, in particular, Minimum Cross Entropy (MCE) principle.

The underlying inference network is decomposed into some small pieces to avoid an exponential explosion of the number of states as the number of variables in the network increases. Each of these pieces corresponds to a Boltzmann-Jeffrey Machine (BJM) which is a highly parallel hypercube-like computational structure for probabilistic reasoning. The beliefs are propagated throughout the network in parallel through the intersections of the BJM's

A Recursive Causal Network Description Language (RCNDL) has been designed and implemented in several machines. One of the interpreters is implemented for Encore Computer System, a memory-shared multi-processor system, based on the concept of parallel thread.

Publications List:

W. Wen, "Parallel MCE reasoning in Recursive Causal Networks", Presented at AAAI-88 workshop on Parallel Algorithm in AI, St. Paul, MN, 8/1988.available as a tech. report (TR 88/15, Department of Computer Science, The University of Melbourne).

W. Wen, "Parallel MCE reasoning and Boltzmann-Jeffrey Machine Networks", in Proc. 3rd IEEE international symp. on intelligent control, Arlington,VA, 8/1988

Contact: Wilson Wen E-mail: wwen@goanna
Department of Computer Science
Royal Melbourne Institute of Technology
Melbourne, 3001
Phone:660-2298

Title of Project: The MR-1 Project

Chief Investigators: Steve Mabbs, Dr Kevin Forward

Institution: University of Melbourne

Starting date and duration: Jan 88, about 1.5 years full-time done, estimate about another 1.5 years till completion.

Funding Sources: None

Number of People on Project (Full Time/Fractional): 1 full-time PhD

Hardware Developed: Multiprocessor architecture using hierarchical memory system. Note: this architecture is being simulated, not built.

Software Developed: Gate-level logic simulator called DIMSIM written in C.

Abstract:

The aim of recent research at the University of Melbourne is to investigate a number of issues related to multiprocessing. A generic architecture, the MR-1 is being simulated to study, inter alia, instruction set optimization and hierarchical memory structures. The MR-1 is specifically being designed to support a real-time version of the UNIX operating system. RISC principles are used to simplify processor design and increase system responsiveness. A hierarchical memory is used along with knowledge about the locality of data references in a program to reduce the incidence of shared-memory contention. However, the use of hierarchical memories increases the context-switch time, due to all the data movement required to swap a process' context into virtual memory. This, in turn, reduces real-time responsiveness and so methods of getting around this problem are currently being looked at. A gate-level simulation package called DIMSIM is being used to simulate the architecture, allowing applications to be run on a cycle-to-cycle basis. Some design parameters may be altered and a new circuit generated to observe any scaling difficulties. Also, in order to assist with the bewildering number of proposals for multiprocessor systems, we have developed a classification scheme, which is used to categorize parallel architectures. We are currently in the process of categorizing about 200 architectures.

Publications List::

"An Overview of the MR-1 Project" submitted to 1989 IEAust Conference on Computing Systems

"A Survey of Parallel Architectures" submitted to 1989 IEAust Conference on Computing Systems

Contact: Steve Mabbs E-mail: steve@mullian.mu.oz
Department of Electrical and Electronic Engineering
University of Melbourne
Parkville VIC 3052
Phone: (03) 344 6714, (03) 344 7436

Title of Project: Monash University Multiprocessor

Chief Investigators: Christopher Wallace, Ronald Pose

Institution: Monash University

Starting date and duration: Began in 1982, on going

Funding Sources: ARGS, ARC, Monash Special Research Grant

Number of People on Project (Full Time/Fractional): 5/3

Hardware Developed: 2 multiprocessor backplanes using our own bus driver and bus protocol designs.

A number of virtual memory modules which do their own page translation

A number of processor boards based on NS32032 processors with our own address translation hardware and bus interfaces

2 I/O adaptors which couple our multiprocessor backplanes to an I/O bus. a dual-ported memory board for our VAX 11/750 which has one port connected to our multiprocessor I/O bus, allowing the VAX to be used as one of the multiprocessors' I/O processors

A bus adaptor to allow a multibus-based I/O subsystem to be connected into our I/O bus. multibus-based I/O subsystem containing a 32032 processor board, disk controller, serial-port board, 2 Mbytes memory. This subsystem runs our I/O software interface.

Other hardware currently under development:

an interbus adaptor to allow transparent operation over a number of our tightly coupled multiprocessors.

A graphics processor/display board which will allow multiprocessor graphics applications to be developed.

A SPARC (as in SUN 4 workstations) based processor board for the system.

A much larger memory module (16Mbytes)

A bus diagnostic and performance monitoring board to enable us to investigate bus protocol performance issues.

Software Developed: Capability-based operating system kernel to run on the multiprocessor hardware. The programming language, "Chi", which tries to take advantage of the persistent objects provided by the kernel.

Other software currently under development: Unix operating system to run on top of the capability-based kernel.

User interface software to make the unusual features of the system easy to use.

Monitor and diagnostic software and emulators for the SPARC based processor being built.

Abstract: (25 lines or less)

This Tightly-coupled multiprocessor project began in the Department of Computer Science of Monash University, Melbourne, Australia in 1982. Hardware design commenced in 1983. We anticipate having a 20 processor system running by the end of 1989.

The system introduces the concept of a global, persistent, virtual memory in which all objects in all systems of this type throughout the world resides. An unusual Password-Capability system has been developed to control access to this large virtual address space. The Password Capability system avoids the difficulties of segregation or tagging which have occurred in other capability-based systems.

A novel hardware address translation scheme has been developed to support the large global virtual address space. Using this scheme the processors generate an intermediate address, and the memory modules themselves translate intermediate addresses into physical memory addresses.

Publications List:

R. D. Pose, M. S. Anderson and C. S. Wallace, "Aspects of a Multiprocessor Architecture", Proc. of the Workshop on Future Directions in Computer Architecture and Software, May 5-7, 1986, Charlston, SC, pp. 293-295.

A. S. M. Sajeev, "Language Constructs for Persistent Object Based Programming", Proc. of the 7th IEEE Phoenix Conf. on Computers and Communications, Scottsdale, Arizona, March 1988, pp. 251-258.

M. Anderson and C. S. Wallace,"Some comments on the implementation of capabilities",The Australian Computer Journal, Vol. 20, No. 3, Aug 1988.

M. Anderson, R. D. Pose and C. S. Wallace, "A Password Capability System", The Computer Journal, VOL 29, 1, 1986, pp. 1-8.

C. S. Wallace, A Physically Random Number Generator",to appear in Computer Systems Science and Engineering.

C. S. Wallace and D. M. Koch, "TTL-compatible multiport bus", Computer Systems Science and Engineering, VOL 1, 1, 1985, pp. 47-52.

R.D. Pose, M.S. Anderson and C.S. Wallace, "Implementation of a Tightly Coupled Multiprocessor", Australian Computer Science Communications, Vol. 9, No. 1, 1987, pp. 330-340.

R.D. Pose, "Capability Based, Tightly Coupled Multiprocessor Hardware to Support a Persistent Global Virtual Memory", Proc. of the 22nd Annual Hawaiian Int. Conf. on System Sciences, Kailua-Kona, Hawaii, Jan 3-6, 1989, Vol II, pp. 36-45.

Contact : Ronald Pose
Dept. Computer Science
Monash University
Clayton,AUSTRALIA 3168.
Telephone: (03) 565 3903
Fax: (03) 565 4746

E-mail: rdp@bruce.cs.monash.oz.au

Title of Project: Centre of Expertise in Distributed Information Systems

Chief Investigators: Professor Andrew Lister, Professor Sjir Nijssen.

Institution: University of Queensland.

Starting date and duration: November 1988 for 3 years

Funding Sources: Telecom Australia

Number of People on Project (Full Time/Fractional): 3/3

Hardware Developed: n/a

Software Developed: n/a

Abstract:

To assist Telecom Australia's development of the software technology for large, distributed, information systems, applicable to information value-added services, network connectivity value-added services (Intelligent Networks), and network management.

To undertake a programme of directed research into the fundamental problems inherent in large-scale distributed information systems.The programme will concentrate on the effective application of software technology to database design and distributed interworking of databases relevant to telecommunication services applications and telecommunications network management.

Publications:

Tim Mansfield, Kerry Raymond, "A Specification in LOTOS of Topor's Distributed Termination Detection Algorithm", Univ Qld Comp Sci Distributed Systems Lab Discussion Document No 2 (13 pages)

Tim Mansfield, Kerry Raymond, "A Specification in Z of Topor's Distributed Termination Detection Algorithm", Univ Qld Comp Sci Distributed Systems Lab Discussion Document No 4 (6 pages)

Tim Mansfield, "Problems with Formal Description Techniques", Univ Qld Comp Sci Distributed Systems Lab Discussion Document No 6 (7 pages)

Kerry Raymond, Tim Mansfield, "Specification of a Distributed System", Univ Qld Comp Sci Distributed System Lab Discussion Document No 8 (7 pages)

Tim Mansfield, Kerry Raymond, "Expressing Liveness Constraints in LOTOS", Univ Qld Comp Sci Distributed Systems Lab Discussion Document No 10 (5 pages)

Contact: Professor Andrew Lister E-mail: dsl@batserver.cs.uq.oz
Key Centre for Software Technology,
Dept. of Computer Science,
University of Queensland,
St. Lucia, Queensland, 4067.
Phone: (07) 377 3952
Fax: (07) 371 0783

Title of Project: A Remotely Accessed Transputer Development System

Chief Investigators: Dr. Tom Hintz, Mr. John Hulskamp and Dr. Wayne Moore

Institution: University of Technology, Sydney
Royal Melbourne Institute of Technology,
Mitchell College of Advanced Education

Starting date and duration: January 1989 - 1991

Funding Sources: internal and external applied for

Number of People on Project (Full Time/Fractional): 3 fractional

Hardware Developed:

Software Developed: Communications package and modifications to development system

Abstract: (25 lines or less)

The system under development provides, at a remote site, the same functionality of a mutli-Transputer development system that would normally be sitting on the desk of the developer. This system is being developed by producing new software and modifying existing software for the INMOS D700D Transputer Development System.

Publications List:

J.P.Hulskamp, T.Hintz, "Transputer-based Research and Development in Australia: Current Status and Future Prospects", International Conference on Applications of Transputers, University of Liverpool, U.K., August 23-25, 1989.

Contact: Tom Hintz
School of Computing Sciences,
University of Technology,
Sydney, PO Box 123,
Broadway, NSW 2007

E-mail: tom@nswitgould.oz

Title of Project: PMS-Prolog - A Multiprocessor Implementation of Prolog with Processes, Modules and Streams

Chief Investigators: Dr. Michael Wise and Dr. Tom Hintz

Institution: Sydney University and University of Technology, Sydney

Starting date and duration: January 1988 - indefinite

Funding Sources: Australian Research Council

Number of People on Project (Full Time/Fractional): three fractional

Hardware Developed:

Software Developed: A parallel version of Prolog using modules

Abstract: (25 lines or less)

The aim of the PMS-Prolog project is the design of a multiprocessor implementation of Prolog based on coarse-grain parallelism. This is the second generation of the system known as EPILOG. EPILOG was the focus of experiments conducted between 1979 and 1986. A fairly standard version of Prolog is running on two processors. A version with "modules" is currently running on a Sun workstation and is being ported to Transputers.

Publications List:

Wise, M. J., "EPILOG: Re-interpreting and Extending PROLOG for a Multiprocessor Environment", Implementations of PROLOG, ed. J. A. Campbell, Ellis Horwood (1984).

Wise, Michael J., "Experimenting with EPILOG: Some Results and Preliminary Conclusions", Thirteenth Annual International Symposium on Computer Architecture, Tokyo, Japan, pp. 130-9 (2-5 June 1986).

Wise, Michael J., Prolog Multiprocessors, Prentice-Hall (Australia) (December 1986).

Contact: Tom Hintz
School of Computing Sciences,
University of Technology,
Sydney, PO Box 123,
Broadway, NSW 2007

E-mail: tom@nswitgould.oz

Title of Project: Parallel Graphics Testbed

Chief Investigators: Dr. Tom Hintz and Dr. Kevin Suffern

Institution: University of Technology, Sydney

Starting date and duration: January 1988 - 1990

Funding Sources: internal

Number of People on Project (Full Time/Fractional): 3 fractional

Hardware Developed:

Software Developed: modification of INMOS raytracing program

Abstract: (25 lines or less)

Realistic image generation is based on a ray tracing program which allows a realistic depiction of three dimensional images such as spheres and planes. Inclusion of "hooks" in the software allow students to add various shading algorithms and to examine such factors as anti-aliasing, refraction and microscopic interactions between light rays and surfaces. Student projects have added cones, cylinders, ellipsoids and bounded planes to the objects which can be rendered. Future assignments will look at user orientated means of input to the object and light source database and comparison of various rendering algorithms as well as alternative algorithms for parallel solutions to the problem. A project to investigate procedurally defined textures is also underway. Textures generation techniques can be roughly classified into two methods - a stored table of values usually obtained from a frame grab from an image captured by a video camera and procedurally defined functions that return a value.This investigation is concerned with synthetic textures that evolve over time and created by defining a simple algorithm for a process/particle to follow. Unlike conventional bombing techniques, the particles will be sensitive to and also affect their environment (2 or 3D space). It appears that this sort of process may be able to bridge the gap between regularity and randomness and produce a whole new class of interesting textures.

The activities in support of this include part of the Occam graphics library has been converted to C. A utility has been written to load and save images from the B007 to the PC. A simple directed bombing process has been implemented.

Publications List:

Hintz, T., A Parallel Architecture Graphics Processor, Austgraph 85, Third Australasian Conference on Computer Graphics, 1985.

Contact : Tom Hintz
School of Computing Sciences,
PO Box 123, Broadway,
NSW 2007

E-mail: tom@nswitgould.oz

Title of Project: Distributed Operating Systems for Dynamic Load Sharing

Chief Investigators: Mark Phillips and Dr. Tom Hintz

Institution: University of Technology, Sydney

Starting date and duration: 1988 - 1991

Funding Sources: Key Centre for Advanced Computing Sciences

Number of People on Project (Full Time/Fractional): 5 fractional

Hardware Developed: Shared memory system based on Transputers

Software Developed: distributed operating system, packet compiler, Ethernet software, packet loader

Abstract: (25 lines or less)

The emphasis on the research to date has been on the communication aspects of dynamic load sharing. The system makes extensive use of Remote Procedure Calls for message passing, and is based on the idea of defining a computer task or process as a series of separate independent packets. A packet is an abstraction based on a single unit of work. Each packet can then be loaded onto a node independently of other packets and depending on the current processing load of surrounding nodes, a packet can be moved about the system.

Publications List:

Phillips, M., A Distributed Operating System, Masters Thesis, University of Technology, Sydney, 1988.

Contact : Tom Hintz
School of Computing Sciences,
PO Box 123, Broadway,
NSW 2007

E-mail: tom@nswitgould.oz

Title of Project: Document Image Processing and Management

Chief Investigators: Dr. Kevin Suffern and Dr. Tom Hintz

Institution: University of Technology, Sydney

Starting date and duration: 1989 -

Funding Sources: Company Teching Fellowship Scheme and a local company

Number of People on Project (Full Time/Fractional): 3 fractional

Hardware Developed:

Software Developed: Compression algorithms in OCCAM

Abstract: (25 lines or less)

Current compression algorithms (CCITT GROUP III & IV) allow monochrome images to be efficiently compressed and decompressed, but efficient and effective algorithms to deal with colour and/or grey scale images are not yet available. The project is to develop efficient and reliable compression techniques which will provide almost instantaneous compression and decompression of these images in a PC workstation; making use of the raw processing power and the parallel architecture and programming environment provided by the Transputer.

Publications List:

Contact: Tom Hintz
School of Computing Sciences,
PO Box 123, Broadway,
NSW 2007

E-mail: tom@nswitgould.oz

Title of Project: Systems and Software Engineering for Parallel Machines Specification and Development of an Imbedded Transputer System Using Data Flow Diagrams

Chief Investigators: John Leaney

Institution: University of Technology, Sydney

Starting date and duration: 1988 -1990

Funding Sources: internal

Number of People on Project (Full Time/Fractional): 5 fractional

Hardware Developed: Robot mouse

Software Developed: Sensor and motor controller and maze solver

Abstract: (25 lines or less)

The IEEE MicroMouse competition requires an electromechanical mouse to explore and then run a maze in minimum time. Mice compete against each other in national and international competitions each year. A formal systems and software specification(using the IDE computer aided software engineering tools) was used to develop the mouse. The data flow diagrams are used as the development tool since there is a one-to-one mapping between data triggered processes on the DFD and channel triggered processes in CSP/Occam.

Publications List:

Contact: John Leaney E-mail: tom@nswitgould.oz
School of Electrical Engineering,
University of Technology, Sydney,
PO Box 123,Broadway, NSW

Title of Project: Formal Specification of a Tennis Court Line Fault Detector using CSP

Chief Investigators: John Leaney

Institution: University of Technology, Sydney

Starting date and duration: 1988

Funding Sources: internal

Number of People on Project (Full Time/Fractional): 2 fractional

Hardware Developed:

Software Developed: Software system for the line fault detector

Abstract: (25 lines or less)

A prototype line fault detector, based on a special ball, a new transducer, analogue signal detection, digital signal processing and pattern matching has been developed. A CSP model of the line fault detector has been developed. Using CSP theory on the CSP model of the line fault detector, the specification and design (including autocorrelations and minimum distance pattern matching) have been shown to satisfy the requirements and to be deadlock free.

Publications List:

Contact: John Leaney E-mail: tom@nswitgould.oz
School of Electrical Engineering,
University of Technology, Sydney,
PO Box 123,Broadway, NSW

Title of Project: Energy Minimization and Parallel Distributed Processing

Chief Investigators: Raymond Lister

Institution: University of Sydney

Starting data and duration: June 1986 - June 1990

Funding Sources: None.

Number of People on Project (Full Time/Fractional): 1

Hardware Developed: None

Software Developed: A few thousand lines of C code, simulating various architectures.

Abstract: (25 lines or less)

A parallel distributed processing architecture has been developed for solving traveling salesman problem. It is similar to an architecture developed by Hopfield and Tank, but it only has log (N) interconnect for each unit, compared with Hopfield and Tank's O(N) interconnect.The approach is a discrete one, and suggests that the capacity of analog approaches to move within the volume of the solution hypercube is not as important as previously thought.

Publications List:

Lister, Raymond "A Discrete Neural Matrix Approach to the Travelling Salesman Problem With Low Connectivity". In press.

Contact: Raymond Lister E-mail: ray@basser.cs.su.oz
Basser Department of Computer Science
University of Sydney
NSW 2006
AUSTRALIA

Title of Project: Construction of Dataflow Multiprocessors - CSIRAC II

Chief Investigators: Dr Greg Egan and Dr David Abramson

Institution: C.S.I.R.O.
Royal Melbourne Institute of Technology

Starting data and duration: June 1986 Ongoing

Funding Sources: C.S.I.R.O, R.M.I.T..

Number of People on Project (Full Time/Fractional): 9/6

Hardware Developed: Message Passing Multiprocessor, SUN Interface, Prototype Dataflow processing element

Software Developed: Simulators, Compilers, Hardware exercisers

Abstract: (25 lines or less)

The RMIT/CSIRO Parallel Systems Architecture Project commenced in May 1986. It is a joint collaborative project between the Royal Melbourne Institute of Technology and the Commonwealth Scientific Industrial Research Organisation, Division of Information Technology. The purpose of the Project is to investigate parallel algorithms, methodologies, languages and architectures, and in particular architectures based on the dataflow model of parallel computation. The variant of dataflow model being studied is that first proposed in 1976 by Egan at Manchester University, UK and subsequently further developed at RMIT. A multiprocessor emulation facility is available for high speed interpretation of the programs as well as a conventional discrete event simulation of the architecture. Compilers for a number of dataflow-like languages are being developed.

The purpose of this project is to build a high speed multiprocessor called CSIRAC II using dataflow processing elements. The target performance for each processor is a sustained diadic node evaluation rate of 5 million instructions per second (MIPS), sustained monadic rate of 10 MIPS, and a sustained diadic vector rate of 10 MIPS.

CSIRAC II has many features in common with other dataflow processors such as the Manchester machine, Sigma-1, Monsoon and QP-1. It differs from other dataflow architectures in the following ways:

- The architecture uses a hybrid static evaluation model with a dynamic model.
- The machine supports vector and list operations
- Graphs are partitioned and the partitions are allocated statically to processing-elements.
- Storage nodes are provided to allow the graph to retain 'semi-permanent' information.
- An Object Store is provided for large structures and persistent objects (e.g.files).

Publications List:

D.Abramson and G.K. Egan, " An Overview of the RMIT/CSIRO Parallel Systems Architecture Project", Proceedings of 1988 Australian Computer Science Conference, Brisbane, Feb 1988. Republished in Australian Computer Journal, August 1988.

D.Abramson and G.K. Egan, "Design Considerations for a High Speed Dataflow Multiprocessor, Proceedings of "Dataflow: A status Report", Prentice-Hall, in print..

D. Abramson and G.K. Egan "The RMIT Data Flow Computer: A Hybrid Architecture", Royal Melbourne Institute of Technology Technical Report, TR-112-057R, 1987. To appear in The Computer Journal.

D. Abramson, G. K. Egan, M. Rawling, A. Young, "The RMIT Data Flow Computer: The Architecture", RMIT Technical Report TR-112-061R, 1987 Royal Melbourne Institute of Technology, Melbourne, Australia..

G.K. Egan, "Data-flow: Its Application to Decentralised Control", Ph.D. Thesis, Department of Computer Science, University of Manchester, 1979.

G.K. Egan, "A Decentralised Computing System Based on Data-flow", Proceedings of the IEEE Industrial Control and Instrumentation Conference, Philadelphia, March, 1980.

G. K. Egan, "The RMIT Data Flow Computer: Token and Node Definitions", RMIT Technical Report TR-112-060R, 1987 Royal Melbourne Institute of Technology, Melbourne, Australia..

M. Rawling, "Implementation and Analysis of a Hybrid Dataflow System", M.Eng. Thesis, Royal Melbourne Institute of Technology, Dec.1987.

Young, A. "Implementation of a Multistage Network for Inconnecting a DataFlow Multiprocessor", RMIT Technical Report TR 112 077 R, Royal Melbourne Institute of Technology, Melbourne, Australia.

Contact: Dr Greg Egan E-mail: rcoge@koel.rmit.oz
Dr David Abramson E-mail: rcoda@koel.rmit.oz
Department of Communication Engineering
Royal Melbourne Institute of Technology
P.O. Box 2476V, Melbourne, Vic 3001.
AUSTRALIA

Title of Project: Parallel Processing Languages

Chief Investigators: Dr Greg Egan and Dr David Abramson

Associate Investigators: W. Heath, Dr K Ramamohanarao, M. Rawling, P. Whiting, N. Webb, S. Wail

Institution: C.S.I.R.O.
Royal Melbourne Institute of Technology

Starting data and duration: June 1986 Ongoing

Funding Sources: C.S.I.R.O, R.M.I.T..

Number of People on Project (Full Time/Fractional): 9/6

Hardware Developed:

Software Developed: Compilers for various parallel processing languages

Abstract: (25 lines or less)

The RMIT/CSIRO Parallel Systems Architecture Project commenced in May 1986. It is a joint collaborative project between the Royal Melbourne Institute of Technology and the Commonwealth Scientific Industrial Research Organisation, Division of Information Technology. The purpose of the Project is to investigate parallel algorithms, methodologies, languages and architectures, and in particular architectures based on the dataflow model of parallel computation model . The variant of dataflow model being studied is that first proposed in 1976 by Egan at Manchester University, UK and subsequently further developed at RMIT. A multiprocessor emulation facility is available for high speed interpretation of the programs as well as a conventional discrete event simulation of the architecture. Compilers for a number of dataflow-like languages are being developed. Work is currently proceeding on the design of processing elements for a high speed multiprocessor.

The purpose of this project is to construct compilers for a number of parallel processing languages. The languages that have been chosen are SISAL, from the Lawrence Livermore National Laboratories, ID from MIT and GHC. A compiler is being constructed for a parallel, dataflow version of Pascal. All of the compilers produce assembler code for the CSIRAC II computer. Some of the compilers also produce code for conventional multiprocessors.

Publications List:

D. Abramson, J-L. Gaudiot, W. Heath, "Parallel Manipulation of Arrays in SISAL", RMIT Technical Report TR-112-078R, 1988, Royal Melbourne Institute of Technology, Melbourne, Australia.

G. K. Egan, M. W. Rawling, "I2: An Intermediate Language for the RMIT Data Flow Computer", RMIT Technical Report TR-112-068R, 1988,Royal Melbourne Institute of Technology, Melbourne, Australia.

W. Heath, "The Implementation of Reduction Merge Operators in Sisal", RMIT Technical Report TR-112-079R, 1989, Royal Melbourne Institute of Technology, Melbourne, Australia.

M. Rawling, C. P. Richardson, "The RMIT Data Flow Computer DL1 User's Manual", RMIT Technical Report TR-112-059R, 1987,Royal Melbourne Institute of Technology, Melbourne, Australia..

N. J. Webb, P. G. Whiting, R. S. V. Pascoe, "Implementing a Functional Language on the RMIT Dataflow Architecture", Proceedings of 12th Australian Computer Science Conference, Woollongong, 1989

P. G. Whiting, " IDA: A Dataflow Programming Language", RMIT Technical Report TR-112-075R, 1988, Royal Melbourne Institute of Technology, Melbourne, Australia.

Contact: Dr Greg Egan E-mail: rcoge@koel.rmit.oz
Dr David Abramson E-mail: rcoda@koel.rmit.oz
Department of Communication Engineering
Royal Melbourne Institute of Technology
P.O. Box 2476V, Melbourne, Vic 3001.
AUSTRALIA

Title of Project: Parallel Application Studies

Chief Investigators: Dr Greg Egan and Dr David Abramson

Associate Investigators: P Beckett, Dr W. Bohm (U Manchester), S Brobst (MIT), P Chang, Dr M. Coulthard (CSIRO), Dr J Feo (Lawrence Livermore National Labs), Dr J-L Gaudiot (U. Southern California), A McKay, M. Ross, Dr M. Rudolph, Dr A Wendelborn (U. Adelaide).

Institution: C.S.I.R.O.
Royal Melbourne Institute of Technology

Starting data and duration: June 1986 Ongoing

Funding Sources: C.S.I.R.O, R.M.I.T..

Number of People on Project (Full Time/Fractional): 9/6

Hardware Developed:

Software Developed: Various Application Studies of Parallel programs have been conducted

Abstract: (25 lines or less)

The RMIT/CSIRO Parallel Systems Architecture Project commenced in May 1986. It is a joint collaborative project between the Royal Melbourne Institute of Technology and the Commonwealth Scientific Industrial Research Organisation, Division of Information Technology. The purpose of the Project is to investigate parallel algorithms, methodologies, languages and architectures, and in particular architectures based on the dataflow model of parallel computation model . The variant of dataflow model being studied is that first proposed in 1976 by Egan at Manchester University, UK and subsequently further developed at RMIT. A multiprocessor emulation facility is available for high speed interpretation of the programs as well as a conventional discrete event simulation of the architecture. Compilers for a number of dataflow-like languages are being developed. Work is currently proceeding on the design of processing elements for a high speed multiprocessor.

The purpose of this project is to parallelise various applications and demonstrate that a speedup can be obtained. A number of different languages and computer architectures are used. Languages range from Pascal (using the Argonne portable tool kit) through SISAL and ID (functional side-effect free languages), Dataflow assembler code, DL1 a dataflow language and Guarded Horn Clauses. Applications conducted so far include Simulated Annealing Optimisation code, Circuit Router (CAD Software), Dataflow graph interpreter, Weather modelling code, Laser range finder object recognition, Robot manipulator control, Parallel compiler (Univ of Adelaide), PDE and Laplace equation solutions and Digital Logic Simulation. New Applications include Image processing and graphics, Genetic optimisation algorithms, Parallel CAD software and Geo-mechanics

Publications List:

Abramson, D. A. "Constructing School Timetables using Simulated Annealing: Sequential and Parallel Algorithms", submitted for publication.

Abramson, D. A. "Using a dataflow computer for functional logic simulation", Third International Conference on Supercomputing, Boston, Massachusetts, May 15-20, 1988.

Abramson, D. A. "Case Studies in Parallel Programming", Presented at International Conference on Computational Techniques and Applications, Brisbane, July 1989.

Abramson D, Egan G. K. ,Rawling M., Baharis C., "The RMIT Dataflow Computer Benchmarks", RMIT Technical Report TR-112-058R, 1987, Royal Melbourne Institute of Technology, Melbourne, Australia.

Egan, G., Webb, N and Bohm, W.. "Numerical Applications on the RMIT/CSIRO Dataflow Machine - CSIRAC II", Proceedings of "Dataflow: A status Report", Prentice-Hall, in print.

Egan G. and Richardson, C. "Manipulator Control Using a Data-driven Multiprocessor Computer System", Invited Paper, Mechanical Engineering Transactions of the Institute of Engineers, Australia, Vol ME10, No 3, Sept 1985.

Egan, G. and Richardson, C. "Object Recognition Using a Data-flow Computing System", EuroMicro Microprocessing and Microprogramming 7, North-Holland, 1981.

Contact: Dr Greg Egan E-mail: rcoge@koel.rmit.oz
Dr David Abramson E-mail: rcoda@koel.rmit.oz
Department of Communication Engineering
Royal Melbourne Institute of Technology
P.O. Box 2476V, Melbourne, Vic 3001.
AUSTRALIA

Title of Project: A Reconfigurable Parallel Processing Board

Chief Investigators: P Drewer, M. Anderson

Institution: Defence Science and Technology Organisation

Starting date and duration: August 1989, Duration 24 months

Funding Sources:

Number of People on Project (Full Time/Fractional):

Hardware Developed:

Software Developed:

Abstract: (25 lines or less)

We are developing a board containing RISC like processors capable of being reconfigured, i.e. parts of their instruction and data paths can be manipulated under program control. It is intended that various programs can reconfigure the board to maximise speedup. The board will support the MACH operating system.

Publications List:

Contact: Dr M. Anderson E-mail: mxa@itd.dsto.oz
Information Technology Division,
ERL, PO Box 1600
Salisbury, 5108
AUSTRALIA

Title of Project: Design and Analysis of a Systolic Architecture for FFT Applications

Chief Investigators: J.P. Hulskamp, Dr J.M. Hawkins

Institution: Royal Melbourne Institute of Technology

Starting date and duration: Started 1987, 4 years

Funding Sources: internal and external applied for

Number of People on Project (Full Time/Fractional): 2 fractional

Hardware Developed:

Software Developed:

Abstract: (25 lines or less)

The need to compute Fourier transforms quickly is often encountered in a number of scientific fields and many instrumental techniques such as nuclear magnetic resonance. The performance of the Fourier transform is usually limited by sequential computing methods, and it is the purpose of this research to develop suitable parallel processing architectures, based on systolic arrays, that overcomes these limits. The application base of this research is the computation of Fourier transforms as used in nuclear magnetic resonance spectroscopy.

Publications List:

Contact: Mr John Hulskamp E-mail: rcojh@gecko.rmit.oz
Department of Communication Engineering
Royal Melbourne Institute of Technology
P.O. Box 2476V, Melbourne, Vic 3001.
AUSTRALIA

Title of Project: Fast Waveform Vector Quantisation using dynamic codebook encoding techniques

Chief Investigators: J.P. Hulskamp,, M.A. Gregory

Institution: Royal Melbourne Institute of Technology

Starting date and duration: Started 1987, 4 years

Funding Sources: ATERB
RMIT Information Technology Board

Number of People on Project (Full Time/Fractional): 2 fractional

Hardware Developed:

Software Developed:

Abstract: (25 lines or less)

This project seeks to develop a signal processing system using parallel processing architectures to achieve reduced data rate communication Techniques being studied included vector quantisation, and dynamic codebook searching, and their implementation on a network of transputers.

Publications List:

M.A.Gregory, J.P.Hulskamp,"Fast waveform vector quantisation using dynamic codebook systolic encoders and its OCCAM implementation" Proceedings of the Australian Transputer and OCCAM User Group, R.M.I.T., Australia, June 23-24, 1988, pp 103-109

J.P.Hulskamp, "Transputer Initiatives for Affordable Supercomputing",Proceedings of the First Australian Supercomputer Conference, A.N.U., December 13-15, 1988.

J.P.Hulskamp, T.Hintz, "Transputer-based Research and Development in Australia: Current Status and Future Prospects", International Conference on Applications of Transputers, University of Liverpool, U.K., August 23-25, 1989.

M.A.Gregory, J.P.Hulskamp, "Simulation of Fast Waveform Vector Quantisation using a dynamic codebook encoder"Proceedings of the Australian Transputer and Occam User Group Conference, 6-7th. July, 1989, pp 21-28, R.M.I.T., Melbourne ISBN 0 86444 163 0.

M.A.Gregory, J.P.Hulskamp, "Simulation of Fast Waveform Vector Quantisation using a dynamic codebook encoder" Submitted for IREECON 1989

Contact: Mr John Hulskamp E-mail: rcojh@gecko.rmit.oz
Department of Communication Engineering
Royal Melbourne Institute of Technology
P.O. Box 2476V, Melbourne, Vic 3001.
AUSTRALIA

Title of Project: Application of Parallel Processing and Transputer Technologies to the numerical modeling of physical systems

Chief Investigators: R. Colman, Dr T. Hintz, Dr M. Coulthard, J.P.Hulskamp

Institution: Victorian Institute of Marine Science

Starting date and duration: 1990

Funding Sources: ARC grant applied for

Number of People on Project (Full Time/Fractional): 5 fractional

Hardware Developed:

Software Developed:

Abstract: (25 lines or less)

The aims of this project are to investigate the inherent parallelism of some existing numerical code of physical systems, to use parts of this code to establish methodologies for major code conversion, to investigate the use of transputers for numerical model simulation running parallel code, and to develop tools to assist software development and provide assessments of configuration strategies necessary for efficient parallel programming based on transputer hardware.

Publications List:

Contact : Mr R. Colman
Executive Officer and Manager, Commissioned Research
Victorian Institute of Marine Sciences
14 Parliament Place
EAST MELBOURNE 3002

Title of Project: Application of Formal Description Techniques to to Parallel Processing with the Transputer

Chief Investigators: J.P. Hulskamp, N.H. Cheng, L.N. Jackson

Institution: Royal Melbourne Institute of Technology

Starting date and duration: Started 1988, duration 3 years

Funding Sources: internal and external applied for

Number of People on Project (Full Time/Fractional): 1 fulltime,2 fractional

Hardware Developed:

Software Developed:

Abstract: (25 lines or less)

The project is aimed at developing a programming environment for the transputer based on Formal Description Techniques (FDTs). This approach allows for the complete and concise specification of the system, and the conformance testing of its implementation. The project adopts the FDT LOTOS (Language Of Temporal Ordering Specification) and automatically generates occam programs to run on the transputer.

Publications List:

N.H. Cheng, J.P. Hulskamp, L.N. Jackson "A Formal Approach to Transputer Software Development" Proceedings of the Australian Transputer and Occam User Group Conference, 6-7th. July, 1989, pp 41-50, R.M.I.T., Melbourne ISBN 0 86444 163 0.

J.P.Hulskamp, T.Hintz, "Transputer-based Research and Development in Australia: Current Status and Future Prospects", International Conference on Applications of Transputers, University of Liverpool, U.K., August 23-25, 1989.

N.H. Cheng, J.P. Hulskamp, L.N. Jackson "The Application of Formal Description Techniques to Parallel Processing with the Transputer" Submitted for IREECON 1989

Title of Project: A real-time infrared imaging system

Chief Investigators: J.P. Hulskamp, C. Lampe

Institution: Royal Melbourne Institute of Technology

Starting date and duration: Started July 1989, duration 4 years

Funding Sources: BHP

Number of People on Project (Full Time/Fractional): 2 fractional

Hardware Developed:

Software Developed:

Abstract: (25 lines or less)

This project is aimed at developing a real-time imaging system, using transputer-based parallel processing techniques, for use in a near infrared imaging system. Such systems have application in thermal imaging for the detection of heat concentrations in hot steel product, and thus will assist in the development of an instrumentation system for the on-line analysis of such product.

Publications List:

Title of Project: Parallelization of Image Processing Algorithms for Natural Scene Analysis and Remote Sensing

Chief Investigators: Anthony Maeder and Binh Pham

Institution: Monash University

Starting data and duration: January 1989; 2 years

Funding Sources: Monash Research Grant

Number of People on Project (Full Time/Fractional): 1/5

Hardware Developed: None

Software Developed: Automatic texture-based segmentation program; image coding programs.

Abstract:

The project is concerned with the development of efficient image segmentation and image coding (for data representation and compression) algorithms which make use of parallelism in various different forms. Specific machines to be used are the Cray X-MP and Transputer. Some investigation of systolic array devices has been undertaken and these form another potential development direction for the algorithms of interest. Change detection in image sequences is highly compute-intensive and requires both segmentation of the images and coding of the changes that occur. Coding for image compression or compaction is also important in view of the large volume of data that occurs in image sequences. Some methods which show promise are prohibitively expensive due to the large amount of scanning or collection of statistics that is involved. In both areas efficient serial algorithms have been developed and these are to be converted to suit the target parallel machines and extended to include compute-intensive refinements that were previously precluded. Significant experience with texture-based statistical image analysis techniques for classification and characterization served as the basis for the block and texture methods used in the serial algorithms.

Publications List: (All associated publications: none on the project directly)

Maeder AJ & Pham B: Overview of techniques for image sequence processing, Monash University Department of Computer Science, Technical Report 87/87 May 1987.

Maeder AJ: Local block pattern methods for binary image compression, Proceedings

of AUSGRAPH 88, Melbourne 4-8 July 1988 p 251-256.

Pham B & Schroeder H: A programmable systolic device for quadratic curve and surface generation, Australian National University, Technical Report TR-CS-88-11 1988.

Sember PP & Maeder AJ: A simple MIMD computer system, Monash University Department of Computer Science, Technical Report 88/120 Dec 1988.

Tischer PE, Maeder AJ & Worley RT: Grey-scale image compression, Australian Computer Science Communications 11(1) Feb 1989 p296-304.

Chong YH, Pham B, Manton M & Maeder AJ: Automatic nephanalysis from infrared GMS data, Monash University Department of Computer Science, Technical Report 89/125 March 1989.

Pham B & Schroeder H: An instruction systolic device for surface generation, Proceedings of COM EURO 89 Conference, Hamburg May 1989.

Pham B, Maeder A: Removal of Navigational Lines from GMS Images, Australian Meteorological Magazine 37 (2) 1989.

Choo AP, Maeder AJ & Pham B: An efficient segmentation algorithm for natural images, Proceedings of the 6th Scandanavian Conference on Image Analysis, Oulu, Finland June 19-22 1989 p1148-1155.

Maeder AJ: Texture characterization using random sampling, in Earnshaw RA, Wyvill B (eds): New Advances in Computer Graphics, Springer-Verlag Tokyo 1989 p603-612.

Pham B, Maeder AJ: Line extraction in grey scale images, Proceedings of AUSGRAPH 89, Sydney July 10-14 1989 p251-257.

Choo AP, Maeder AJ & Pham B: Image segmentation for complex natural scenes, submitted to Image and Vision Computing.

Schroeder H, Schimmler M, Pham B, Maeder AJ & Kunde M: Systolic implementation of local operations in image processing (in preparation).

Contact: Anthony Maeder
Department of Computer Science,
Monash University,
Clayton 3168

E-mail: ajm@bruce

Index

Project Titles