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Data Driven Packet Switch Networks

A 2 x 2 Data Router.

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DATA DRIVEN PACKET SWITCH NETWORKS.

Introduction.

Computer architecture as we know it in our day to day contact with digital computers is based on the Von Neumann Model, where program operation proceeds in a serial fashion usually under the control of a program counter. The computer program controls the execution of machine operations in a sequential manner, however for some time it has been acknowledged that in certain applications where there is a characteristic of parallelism, the conventional Von Neumann type architecture is not ideally suited. Parallel processing using multiple processing elements provides a means of improving system performance by exploiting the in built parallelism of certain problems.

One type of parallel processing architecture being investigated within the Department of Communication and Electronic Engineering at R.M.I.T. is the Data-Flo concept, where multiple processing elements execute programs by means of a data driven mechanism where-by each processing element preforms a pre-defined function as soon as it receives the necessary data packet or Token. The Token, as well as containing the data also carries the processing element number where the computation is to take place and the type of Process (addition, multiplicatiom, etc.) as defined by the node number. Due to the conceptually high number of processing elements required to ensure program parallelism a need arises for a means of high speed communication between processing elements, such a communication network may at first seem a trivial exercise until one considers

a data-flo machine consisting of 128 processing elements each having a 16-bit input and output data path and each being able to communicate with any other element. The problem is reduced to managable proportions if one considers a modula approach where the communication network is based on one fundamental building block, which can be used singularly to connect two processing elements or in large numbers to connect many elements, such a building block is the 2 X 2 Routing network shown in figure 1.

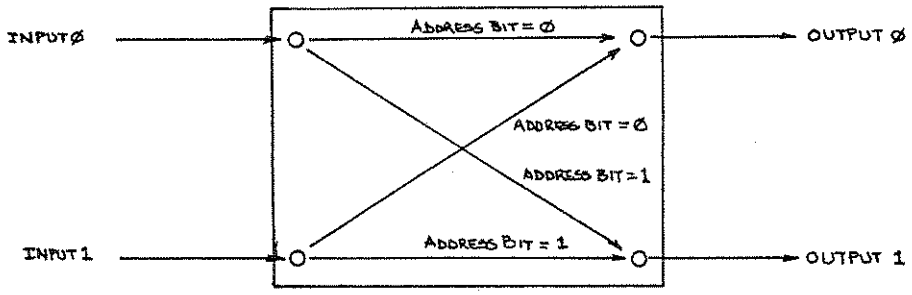

FIGURE .1 2 x 2 Router Network.

The diagram shown in figure 2, demonstrates how these individual networks can be combined to produce a complex communication path between, in this case 32 processing elements.

The N x N Routing Network.

The purpose of this document is to descibe the preliminary work being done towards realizing a compact, fast 2 x 2 Routing network which will provide the basis of my Master Of Engineerig Degree. The router is a data driven switch which receives packets at its two input ports and directs them to one of the two output

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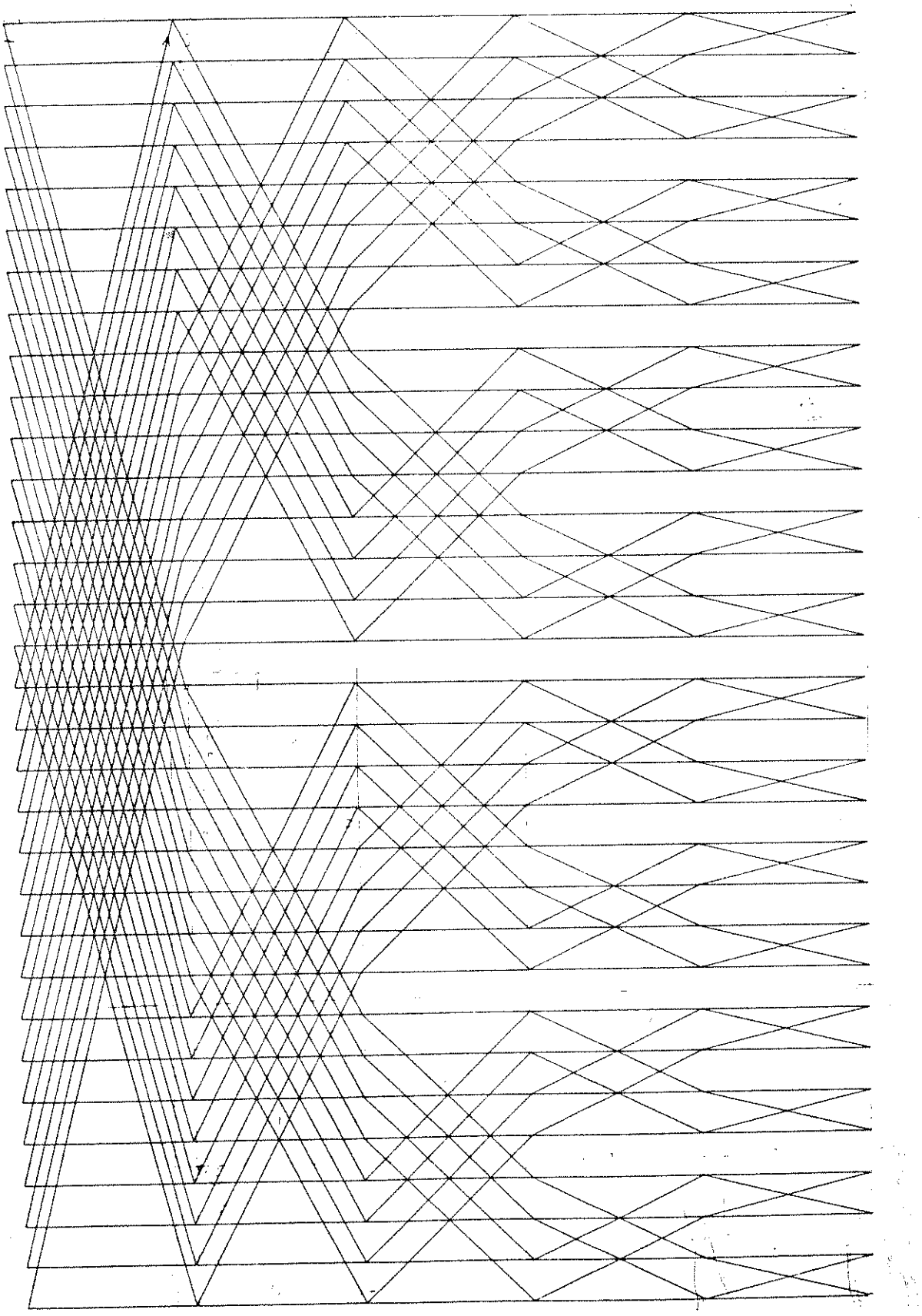
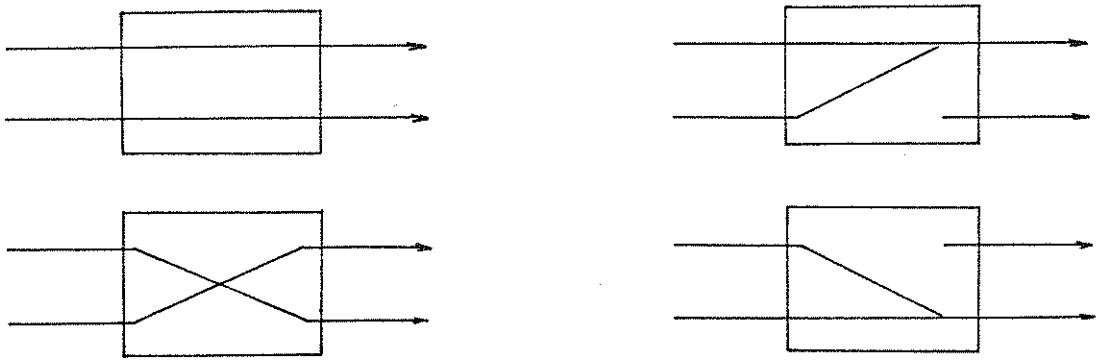
A-G 8° input = 60



ports. The address of the output port to which the data is to be directed is contained within the packet itself, the router operates in a non- blocking mode as shown in figure 3(a), or in the blocking mode in figure 3(b).



(a) Non-Blocking. (b) Blocking.

FIGURE .3

Processing of incoming packets proceeds concurrently where address decoding takes place to determine the destination port. Arbitration cicuitry resolves conflicts between output requests, while two control lines enable data transfers from the previous router or processing element output. The arbitration design is central to the operation of the router and must be able to cope with Metastable States. These states may occur when simultaneous requests are made for the same output port causing the port request latches to assume an undefined electrical state; being neither a logical 1, or Ø. This state should be detected and exception processing enabled to allow the port request to be disabled until the metastable subsides. Figure 4 is one example of an arbitration circuit where the 74LS6Ø provides the metastable state detection.

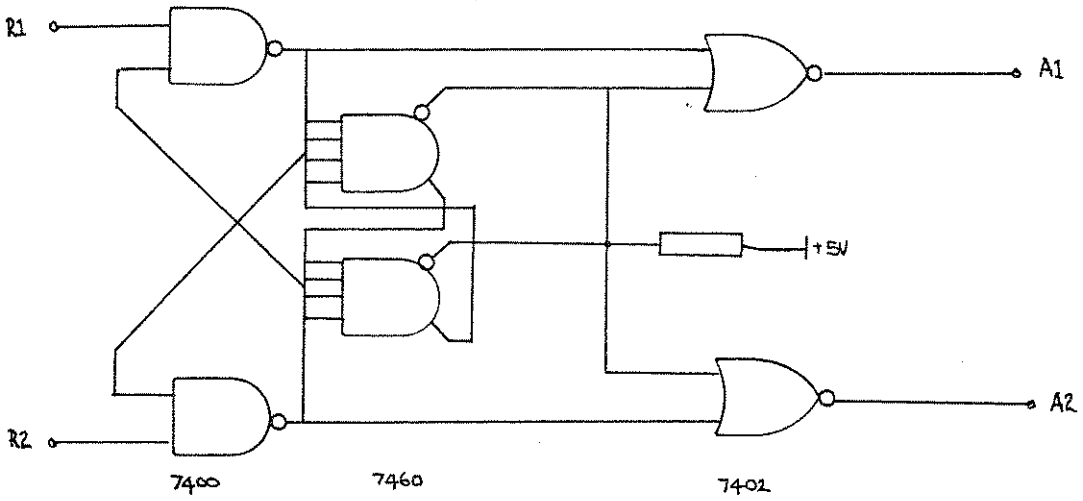


FIGURE .4 Arbitration Circuit.

The design of the 2 x 2 router is by no means trivial, although in itself it does not represent a Masters project, what does however is the implementation of the router so that it can be used in large packet routing networks. The major consideration thus becomes the physical size of the basic 2 x 2 module since the number of modules required is determined from the equation:

$$n = \mathrm{Log}_2 N \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (I)$$

where n is the number of stages and N is the number of inputs and outputs to the network. Thus for any given network size it would require (N x n)/2 router modules, or for example a 32 element machine would require (32 x 5)/2 = 8Ø modules as is shown in figure 2. A conventional design using standard MSI chips would require a minimum of 12 chips per 2 x 2 router module, one approach then is to implement the entire router module using VLSI (Very Large Scale Intergration.)

fabrication in NMOS. It is feasible if not practical to construct the entire 2 x 2 router on a single chip, the problem being that with two sixteen bit input buses, two sixteen bit output buses, associated data flow control lines and power and ground lines a total of 74 pins would be required. The more practical solution is to partition the router along the lines shown in figure 5 and implement each element seperately.

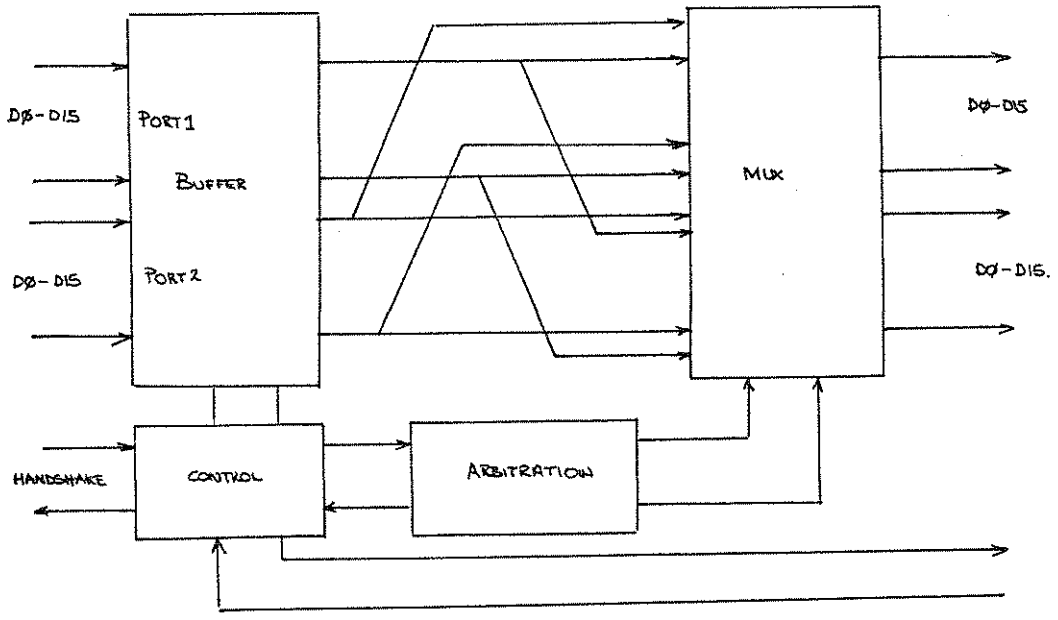


FIGURE 5. 2 x 2 Router Partitioning.

A completely different approach to the scale reduction problem is to Hybridise the router using standard MSI Die, the obvious advantage of this technology over VLSI is in its lower cost. The cost of producing a VLSI chip is of the order of $3000-5000, even as part of a Multi-Chip Project where several designs occupy the same substrate, compared to a cost of several hundreds of dollars to produce a Hybrid circuit.

Fortunately both means are available within the Department allowing the implementation using both fabrication techniques. This will allow a reasonable assessment to be made concerning the desirability or otherwise of each technique with respect to the overall aim which is the development of an 8 element data-flo machine of which the router networks are an essential part. The modification and re-design of the existing Data-Flo processing element is being carried out in conjunction with the development of the router. The element is based on the Motorola MC68000L10 16/32 bit microprocessor supported by 64k words of dynamic read/ write memory expandable to 256k, with 8k words of read only memory and two 1k FIFO's which act as the input and output buffers to the communication network. Data is capable of being read out of the buffer at a rate of one word every 150nS (worst case), with the 2 x 2 router having a through-put design specification of 1 word every 100ns.

Progess towards the implementation of the router is proceeding, although the re-design of the processing element has taken priority since this will support other research areas. The design timetable is to have the new proceesing element built and tested by december '84, with eight boards being conctructed and ready to use in early '85, at this point the development of the routing module should be at a point were a multi-element Data-Flo machine can be demonstrated. The router module should be implemented in both technologies by the end of '85 allowing perfomance analysis to be carried out using the eight element machine.

References

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