OPTICAL COMMUNICATIONS FOR DATA-FLOW

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DESIGN 3 PROJECT
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CONTENTS

ABSTRACT

This design manual describes the design of an experimental optical communication system for a data flow computer. The requirements of such a communication system are presented, and the means and extent to which this design meets these requirements are discussed. Experimental results to date are given. Finally, future enhancements, improvements and expansions, particularly the use of the optical network in a large data flow system, are discussed.

I. INTRODUCTION

Data flow is a parallel processing computer architecture that is starting to gain acceptance as the limitations in speed and performance of conventional von Neumann systems become more apparent and more limiting. A data flow system consists of a large number of processing elements (processors) working on a problem simultaneously. The system functions as quickly as it can pass data from one processing element to another, and so the ultimate performance of any data flow machine is heavily dependant on the performance of its communications structure. Some papers concerning the design of data flow machines give a detailed description of the communications structure required [1,2], while others [eg 3,4,5] do not go into very much detail; this is because it is a difficult problem to solve. Although sometimes treated as if it can be added on as an afterthought, the communications structure is actually a critical part of the design of the data-flow system.

The major problems encountered in designing a communications system for data flow computers are:

(1) maximising data transmission speed,

(2) handling contention when two processors want to send data to the same processor,

(3) maximising the number of paths that can be used at any one time ie. maximising parallelism in the communications structure as well as in the processing structure,

(4) minimising physical connections between processors, so that processors can be added and

removed easily.

(5) keeping cost to a minimum, and

(6) avoiding over-complexity

The optical communications structure around which this design is based [6] automatically satisfies requirements (2), (3) and (4), since there is a unique path from each processor to every other processor, and there is no electrical connection required between processing elements. The structure does require, however, that the processing elements, or at least the communications part, must be fairly accurately aligned with each other and therefore mechanically connected in a rigid frame. Requirements (1), (5) and (6) are not so well catered for, and the implications of this will be discussed later in the paper, as well as possible solutions. This optical structure would be best for large systems, say 100 processors upwards. For these systems, electrical data communication becomes extremely difficult because of the wiring problems. The optical system is, in theory, free from such problems, and so its advantages should outweigh its drawbacks in a large system [6]. This idea is expanded later in the paper.

II. GEOMETRY AND OPTICS

The concept this design is based around is that of providing a free-space optical data link between processors. The processors are arranged in a square grid, and each processor can produce, by some means, a directed light beam to every other processor (Fig. 1). The light beams produced by the processors' transmitting devices reflect off a mirror suspended over the

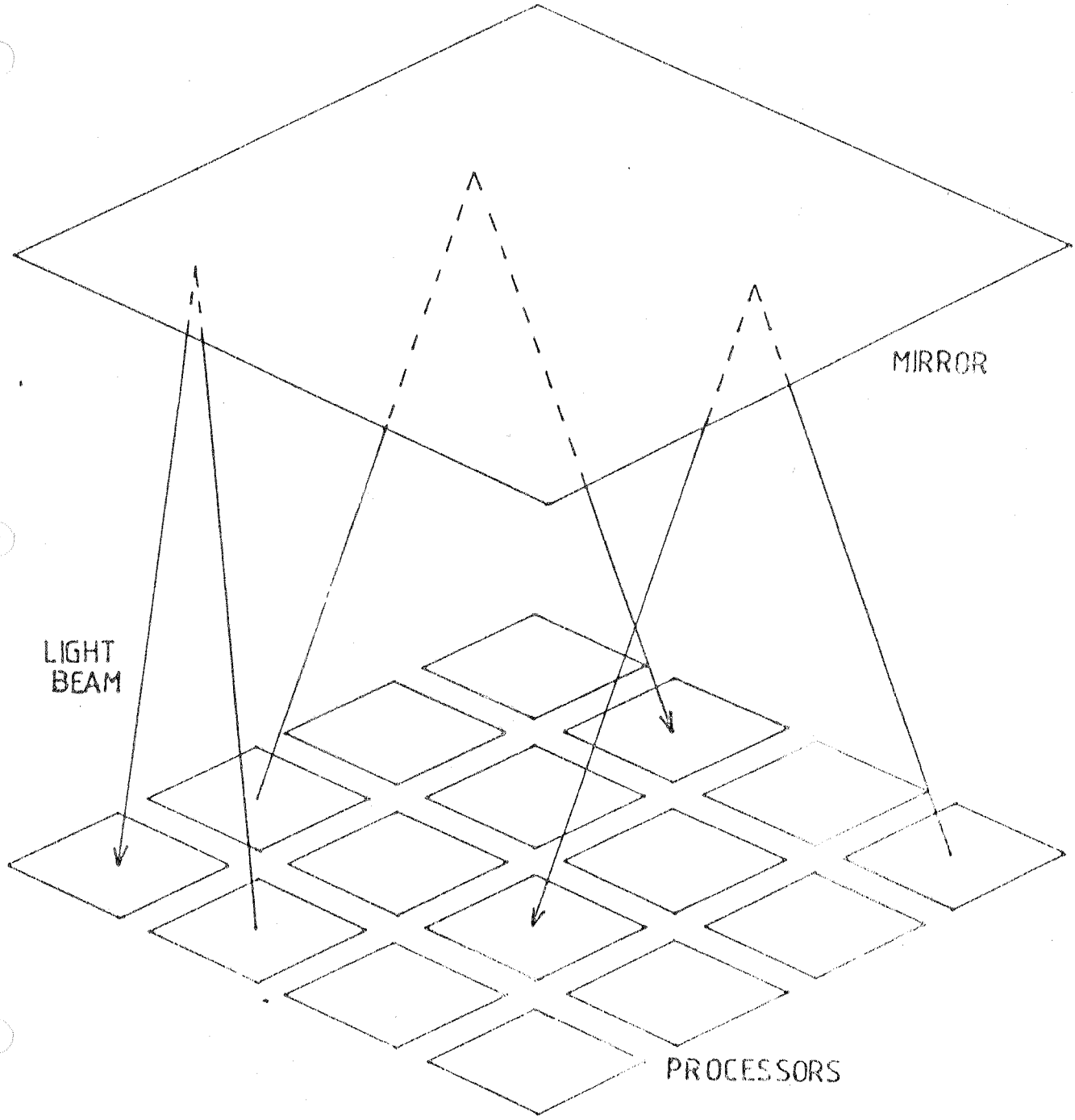


Fig.1 The Optical System

array of processors to reach their destination. This light beam is modulated to pass the data from one processor to another. Thus each processor can send information to any other processor, and every information transfer is independent of every other one, allowing many transfers to take place simultaneously. In addition, if every processor has n optical detectors instead of just one (n being the number of processing elements in the optical network), and by using an appropriate optical layout (Fig. 2), the processor on the receiving end of an information transfer can determine directly which processor is sending the information simply by determining which detector is being illuminated. More importantly, on every processing element there is now an independent receiver for every transmitter that can send to it, and so the contention problem (several processors transmitting to the same receiver) is reduced to one of communications protocol. When a processor wishes to transmit data to another processor, it sends a request signal, waits for an acknowledge signal and then transmits the data. The receiver must have a rapid means for detecting a request signal, determining where it came from and sending an acknowledge back to the source. It must also have some means for arbitrating between simultaneous requests.

There are several means of producing the directed light beam as described. The most desirable would be a vectored laser, as this could provide high speed communications and very low error rates due to the high signal to noise ratio (laser intensity to ambient light intensity ratio). This would enable operation in normal lighting conditions, assuming an open frame

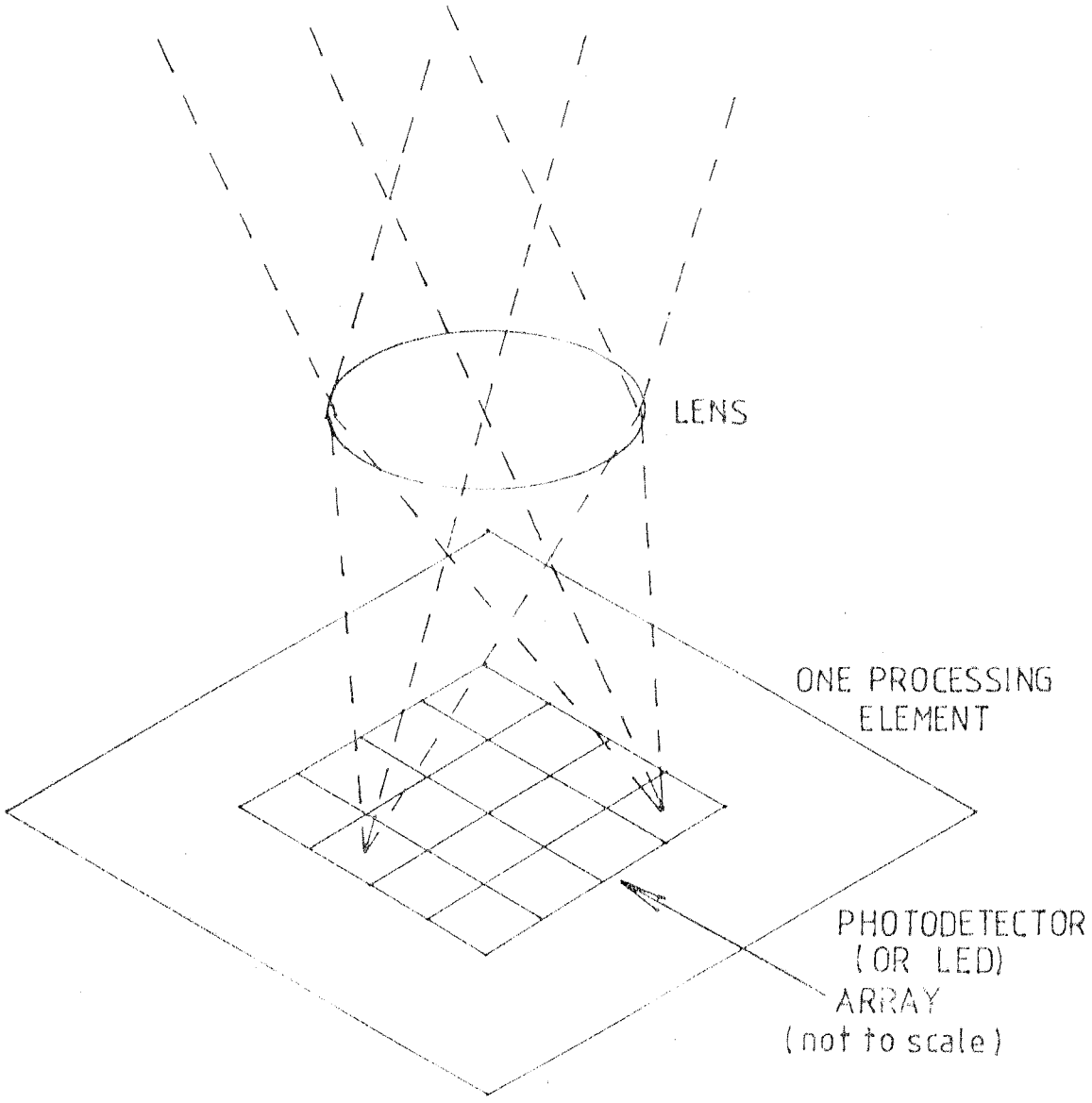


Fig. 2 Array Optics.

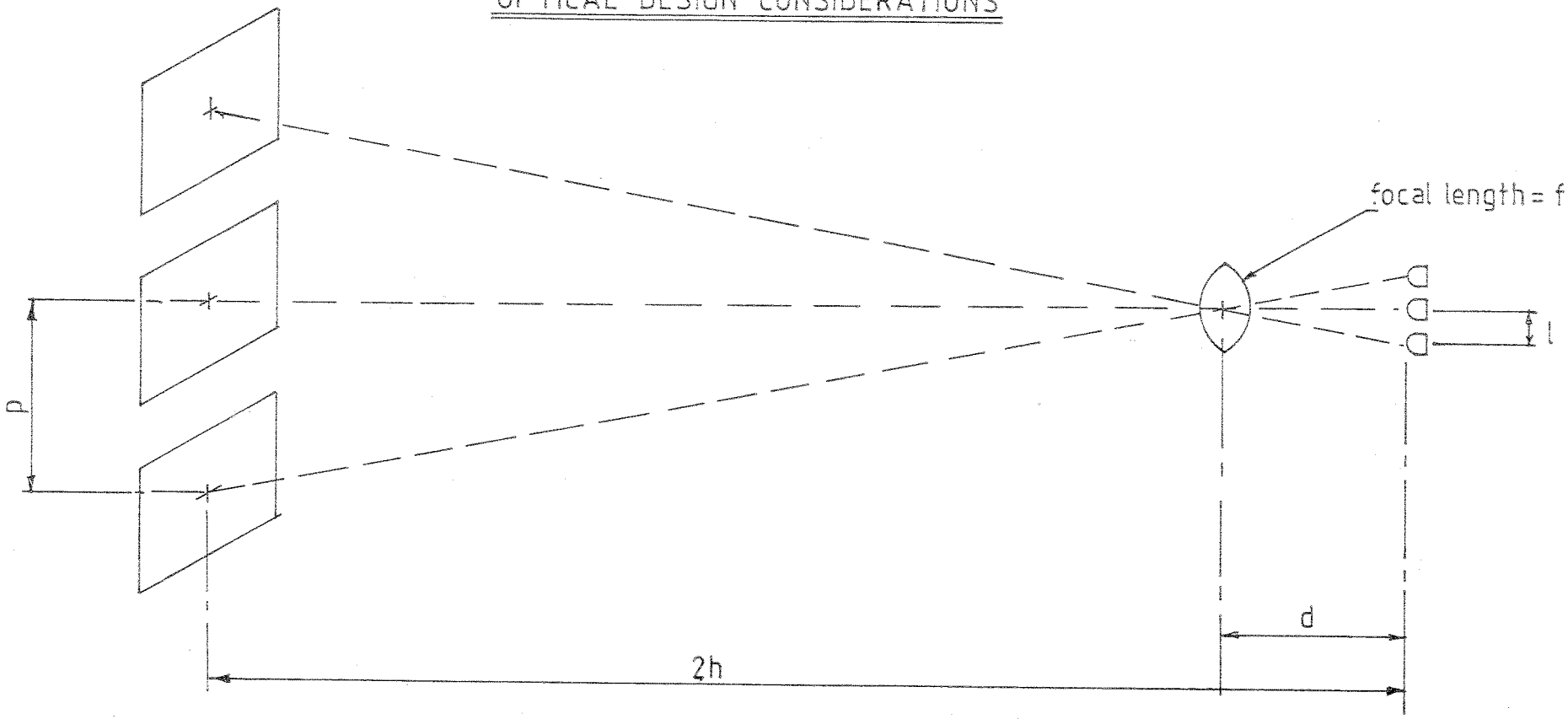
structure was used, as in the prototype. Some means must be found to accurately deflect the beam in the correct direction, and the device used must be fairly small, very rapid in operation, and not be too expensive or complex in prototype form. An extensive literature search was conducted to attempt to find a suitable laser scanning technique to implement in a prototype. Mechanical scanning techniques were eliminated due to their unacceptably slow response (milliseconds), and the only remaining methods are, fundamentally, electro-optic or acousto-optic [7]. Electro-optic devices, which rely on a variation in refractive index of a crystalline substance to produce a deflection or modulation of the laser beam, looked promising initially, as the wide diversity of forms gave the impression that some suitable form could be found to cater for any application. It was found, however, that all realisations were either too limited in their scanning ability, were too bulky or they required high voltages (over 100V was considered undesirably high). For these reasons, it was decided that this type of device was unsuitable for a prototype. Acousto-optic devices [8] can easily produce the required deflection and resolution, but are generally fairly bulky and many also require high voltages. The most promising is a device using ultrasonic waves in a solid medium to produce an apparent diffraction grating that deflects the laser beam, but even these are relatively large, and they also require precisely manufactured transducers and fairly expensive crystals for the diffracting medium, making them inappropriate for this application. Whatever technique is used, further problems arise in the actual

implementation of a vectored laser system as the deflecting devices must be calibrated in the final unit so that the beams end up in the correct positions. This could be a difficult and tedious process, since each deflection increment on each communications unit may have to be set up separately. For a large system, an integrated beam switching device based on electro-optics would probably be an attractive option.

An alternative to a single deflected beam is to use an array of directed beam sources. Instead of producing the beams with a deflection device, every different beam could have a separate source, only one of which is activated at any time. The beams are directed such that each beam falls on a different receiver lens, and the beam sources are arranged in an array that corresponds to the array of processors. This can best be done using an array of light emitting diodes (LEDs) and a lens, which results in the transmitter optics being identical in form to the receiver optics, and the layout is as shown in Fig. 2. The lens focusses the light from the LED into a fairly narrow beam. It is not necessary that the beam be focussed finely enough so that it only strikes one of the detectors in the receiving array - the receiver lens takes care of that - but only to ensure that the fringe of one beam does not fall on an adjacent receiver lens. The direction of the beam emerging from the transmitter lens is dependent on the position of the LED below the lens. The array of LEDs thus produces an image at the plane of the receiver lenses such that one LED image falls exclusively on one receiver. The detailed optical design consists of choosing values for a set of parameters such that

the equation shown in Fig. 3 is satisfied. This equation has a number of variables and has no unique solution, and so values must be chosen sensibly to produce a reasonable design. If the lenses used for the transmitter and receiver have the same focal length, the optical-mechanical design reduces (approximately) to three planes- one containing the processing element printed circuit boards (or more accurately the active surfaces of the LEDs and photodetectors), one containing the lenses, and one containing and consisting of the mirror. The design was finalised with a mirror height of 1.1m, lens focal length of 10cm, spacing between board centres of 20cm, spacing between LEDs and between photodetectors of 1cm, and lens height of 10.5cm. Substituting these values into the equation shows that it is in fact not satisfied, which results in slight de-focussing of the incoming beam. This is actually desirable as it eases alignment and beam non-uniformity problems. A frame was designed and constructed from aluminium extrusions, and it was made so as to enable some adjustment of the height of the lens plane above the PCB.

OPTICAL DESIGN CONSIDERATIONS



$$\frac{1}{f} = \frac{(p+l)^2}{2phl}$$

$$\frac{d}{} = \frac{2hl}{p+l}$$

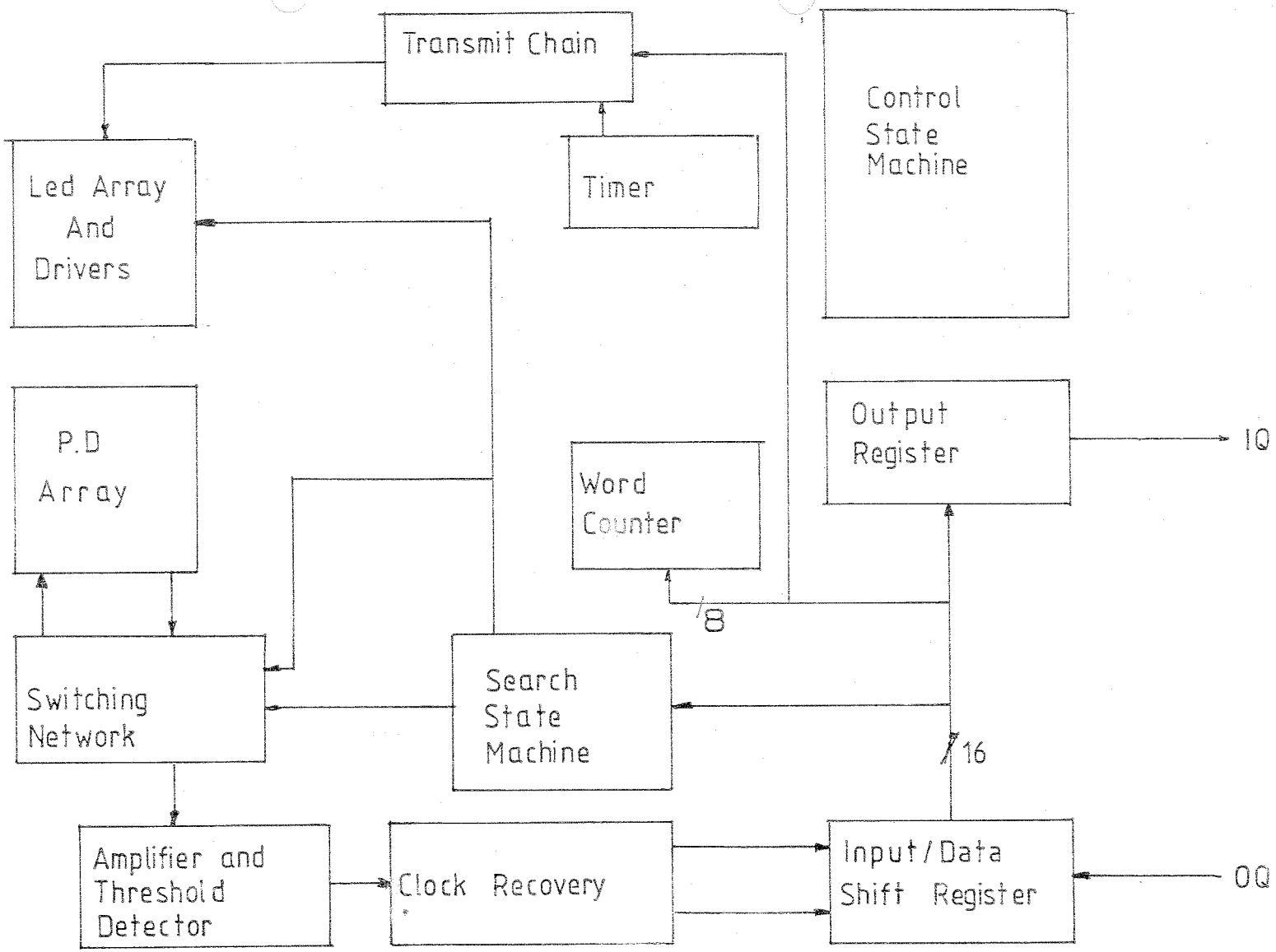
p = processor board spacing
h = height of mirror above l.e.d plane
d = l.e.d lens distance
l = l.e.d spacing

FIG 3

III. CIRCUIT DESIGN

For this prototype, it was decided to construct a (potentially) 4x4 system, containing up to 16 communications boards. This makes the circuitry for selecting the LEDs and photodetectors fairly simple, as all replications are in powers of 2. The LEDs chosen were Hewlett Packard HLMP-3750 ultra bright red LEDs, which have a high intensity output and turn on and off times of about 100ns, giving a potential data rate of the order of 5Mbits/sec. The photodiodes are HP5082-4220 PIN photodiodes, with a response time under ideal conditions of 1ns. In this application, this response time is not achievable, as the illumination from the LED spreads over the edge region of the photodiode, giving a response time of about 300 nanoseconds (see data sheets). The LEDs are driven by a series of transistors to select one out of the array, and to produce the modulated signal. The photodiodes are connected to an amplifier/threshold detector through an array of analog electronic switches, which allows the monitoring of one photodiode at a time for data reception, or several at a time for detecting requests from an unknown source.

The approach taken with this design was to implement all the functions as functional blocks (LED and photodiode arrays, data shift register, output register, word count register and so on) and control them with a finite state machine (Fig. 4). This approach allowed flexibility and the ability to alter the actual operational sequence of the unit after it had been built. The state machine is implemented in the prototype using EPROMS to



SYSTEM BLOCK DIAGRAM

FIG 4

allow it to be commissioned.

The operation of each functional block will be described here and then the sequential operation of the overall unit will be detailed.

The data shift register (see Fig. 5) is a 16 bit register consisting of two 8 bit registers which can be loaded synchronously or asynchronously or shifted left. Only the synchronous load and left shift modes are used. The parallel input data to the shift register comes from the data flow processing element, and the output of the shift register is connected to the output register, the word count register, and the preamble detect. These will be treated in turn. The output register is the data output to the data flow processor, and is loaded whenever the bit counter reaches zero. Data is passed to the processor by a handshake operation performed by the control state machine. The word count register is a presettable counter which counts the number of words remaining to be sent or received. It is loaded under control of the main state machine from the shift register output, and is decremented when the bit counter reaches zero. The load of the word count register also loads the destination address into the flip-flops of the finder state machine. The bits loaded into each register are shown in Fig. xx. The preamble detect is a four bit comparator, which detects a bit pattern of 1011, the end of the preamble. It operates continuously, giving a preamble detect every time that pattern occurs, but it only has an effect if the circuitry is in a state to accept it. The data encoder chain (see Fig. 6) provides the request, acknowledge and preamble functions as

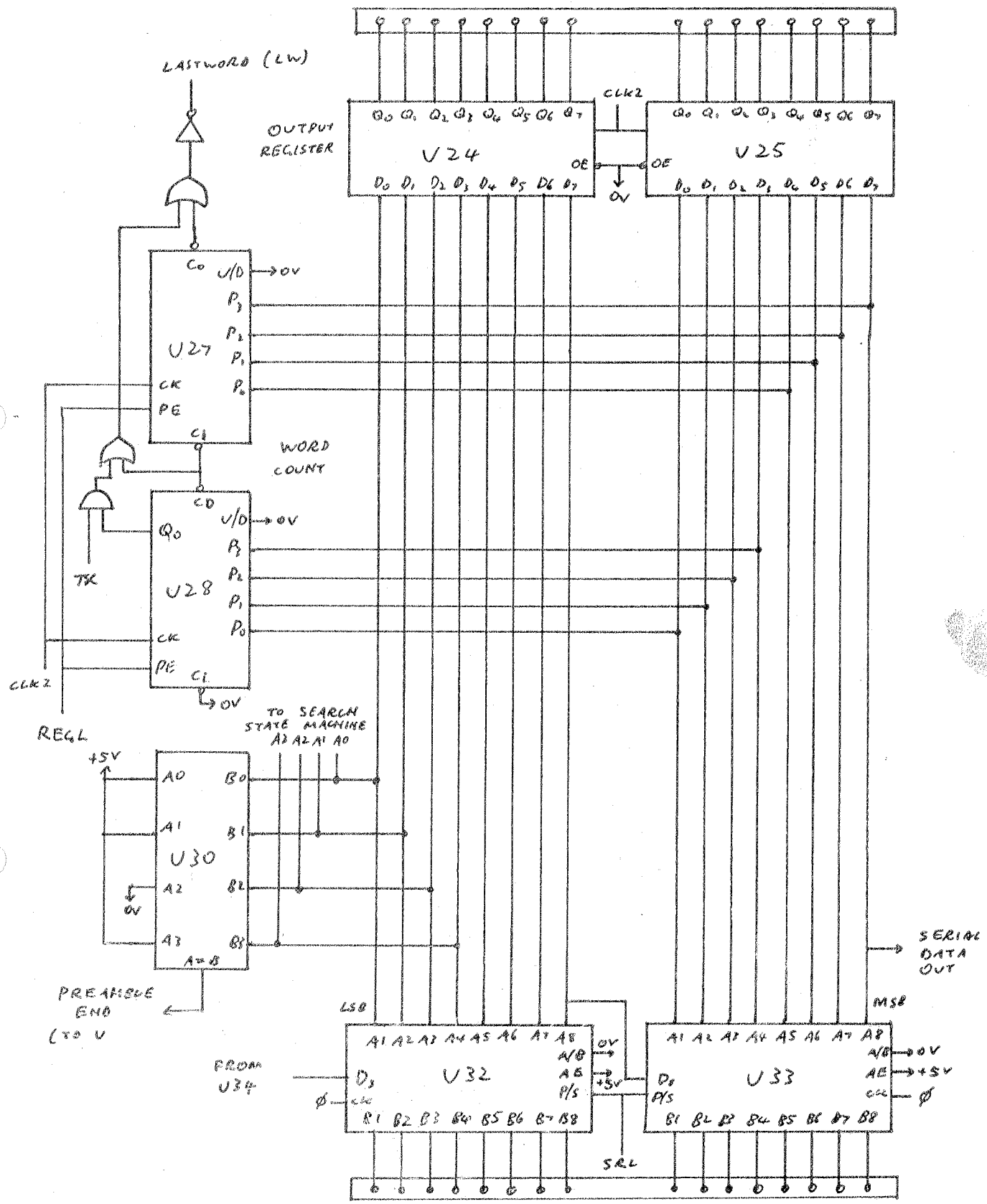


FIG 5 DATA PATH

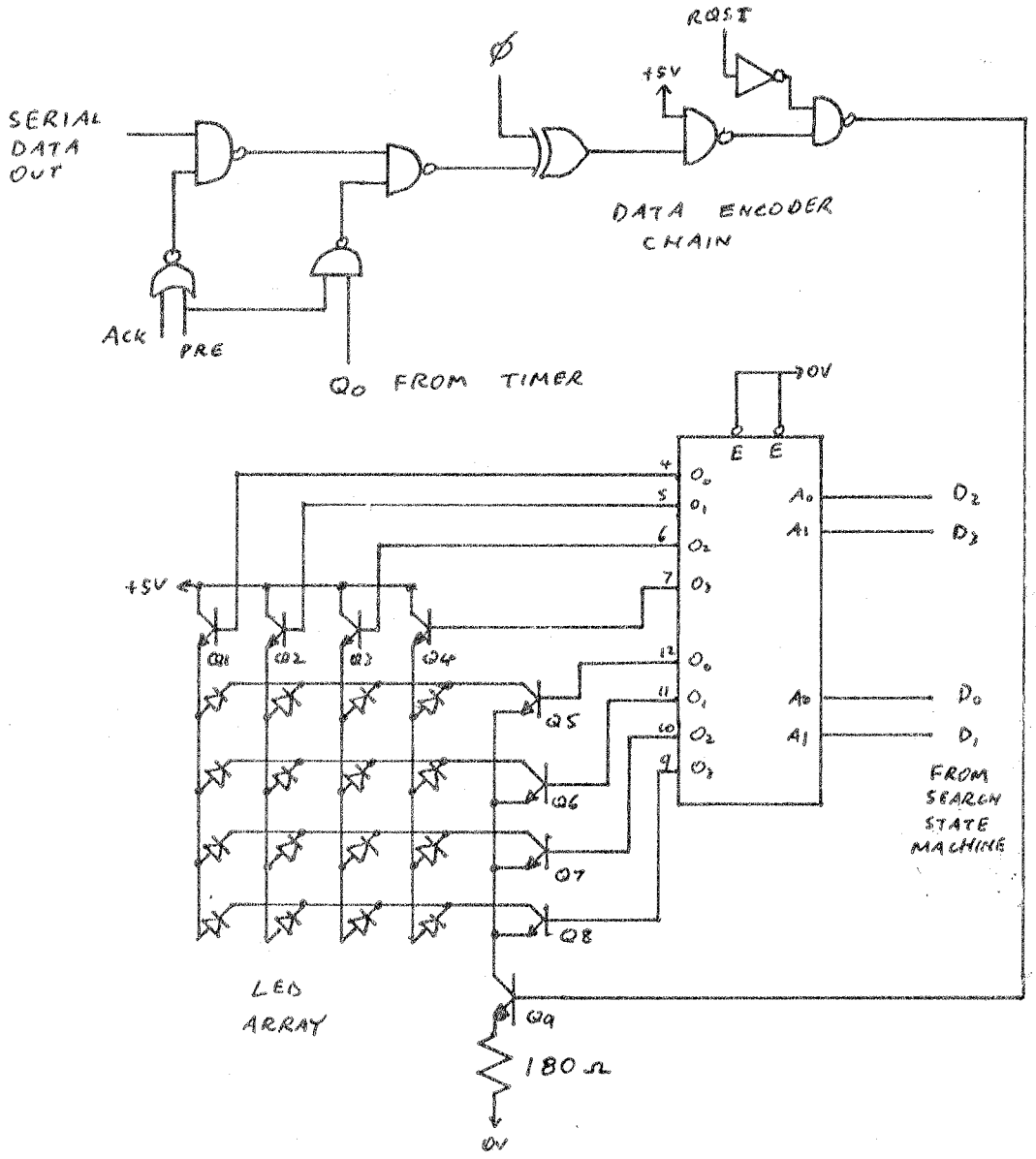


FIG 6 CODING AND TX

well as performing Manchester encoding of the data. A request is a steady on state, which is distinguishable from any other signal sent: Manchester encoding produces a transition for every bit. Preamble and acknowledge are represented by encoded bit streams, preamble being 1010...1011 (16 bits) and acknowledge being a continuous string of 0's. Neither of these bit streams are unique but they are identifiable in their context. It is possible that other signals may be interpreted incorrectly as a preamble or acknowledge, but if this does happen the protocol has already been violated and the system is in a non-functional state. The misinterpretation of data streams as preamble or acknowledge therefore cannot actually cause a system breakdown. The preamble bit stream is generated from the least significant bit of the timer counter.

The bit counter is a 4 bit counter (see Fig. 7) which is clocked on the negative edge of the clock. It is reset when a flip-flop (FF1) is reset, but otherwise it counts. FF1 is reset by a signal from the state machine (RF1), and set by the acknowledge for the handshake controlling the output queue of the processing element. These signals synchronise the state machine and the bit counter. To synchronise the receiver's and transmitter's bit counters, the flip-flop is set by the preamble end detect.

The timer consists of a presettable and resettable 4 bit counter with a logic gate to detect maximum count which provides a control signal to the state machine and disable the timers clock to leave it in the maximum count state. It is reset to provide a fixed time of 15 cycles or preset to load a random

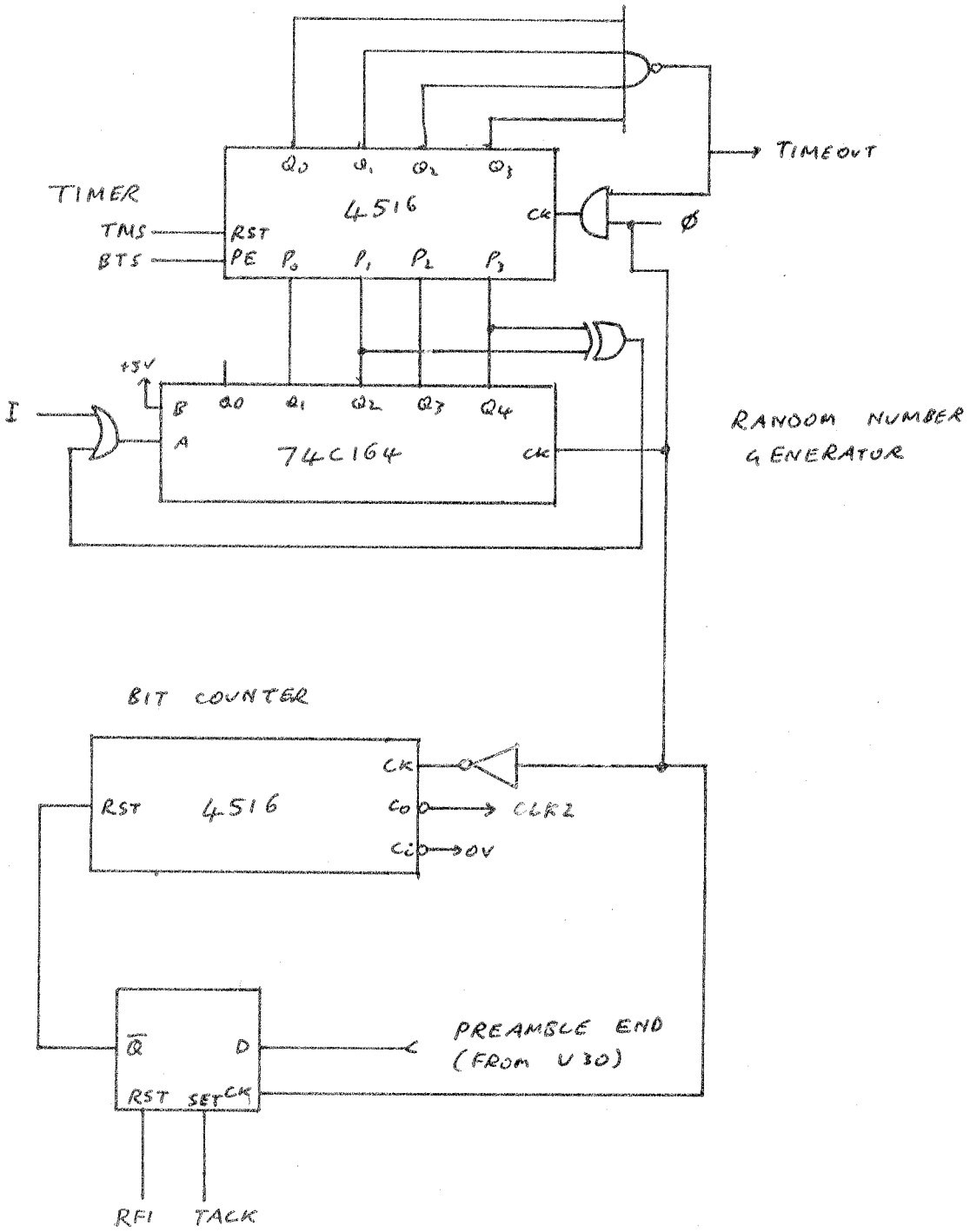

TIMER
TMS
BTS
RST
PE
4516
TIMEOUT
CK
Ø
+5V
I
B
A
74C164
RANDOM NUMBER GENERATOR
BIT COUNTER
RST
4516
CK
CO
CLK2
CI
0V
PREAMBLE END (FROM U30)
RST
SET
CK
RFI
TACK

FIG -7

number for backoff timing.

The random numbers are produced by a standard 5 bit pseudo-random number generator, having a sequence length of 31 bits. In the early prototype stages, a constant number (hard wired) is used to reduce parts count.

The finder state machine (see Fig. 8) implements a binary search scheme. In the initialised state, all photodiodes are connected in parallel by analogue switches and so any incoming signal from any source will be detected. When a signal is detected, it enables the finder state machine. On the next cycle, half of the photodiodes are disabled, and if the signal disappears the bit in the state machine output address controlling which half is selected is inverted: the half containing the active photodiode is thus selected at the end of the cycle. This is then repeated for the remaining half and so on until only one photodiode remains selected. In some ways this process is similar to the successive approximation procedure used in analog to digital conversion. In practice there are few difficulties with the implementation of this scheme. For example, if a spurious request occurs, the state machine will still give a "found" indication, but there will be no incoming signal, and the system will fail. To guard against this, the state machine restarts if there is no signal present when it finishes its search. A fairly large logic network is required to perform the sequential and decoding functions, about 14 packages for a 4x4 network. For a large system, this network would need to be implemented as an integrated device, probably on the the same substrate as the LEDs and photodiodes (see later discussion

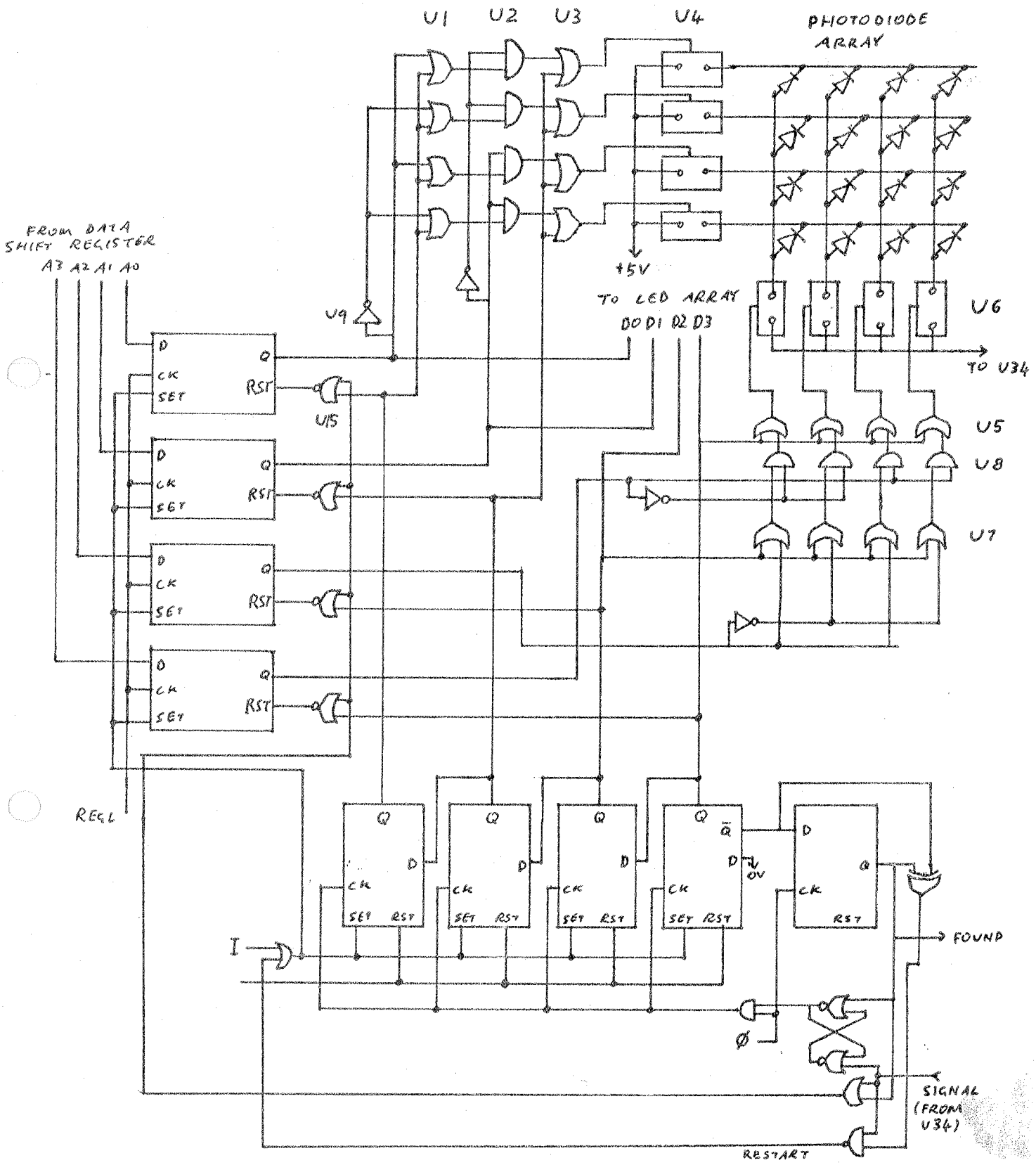


FIG 8 RX AND SEARCH STATE MACHINE

on monolithic fabrication of the arrays).

The remaining circuitry (see Fig. 9) is the photodiode amplifier, acknowledge detect and clock circuitry. The photodiode amplifier simply consists of a voltage comparator, the voltage being derived from the photocurrent passed through a resistor. This simple scheme may be used because the signal levels are quite high. There is an additional resistor from the photodiode to ground, which performs the threshold function. It "bleeds" a small fixed current to ground so that a certain amount of current out of the photodiode is required to produce a detectable signal, and thus protects the amplifier from responding to ambient light levels. The signal from the comparator is processed by a clock regenerator to recover timing information from the Manchester encoded waveform. This processing consists of a differentiator and a monostable. The differentiator produces a pulse at every transition of the input signal, and this triggers the monostable. The monostable is non-rettrigable and has a period of about 0.75 of the clock period, and this combination gives simple timing recovery and rapid synchronisation (see Fig ss). The output of the monostable is the received clock, and this feeds into the clock generator. The clock generator produces clock pulses for when there is no received clock, and the system allows a clock tolerance of +/- 25%.

The acknowledge detect function is performed by a retriggerable monostable and 2 bit counter. The period of the monostable is 75% of a clock period, and during a continous sequence of 1's or 0's its output remains high. While its output

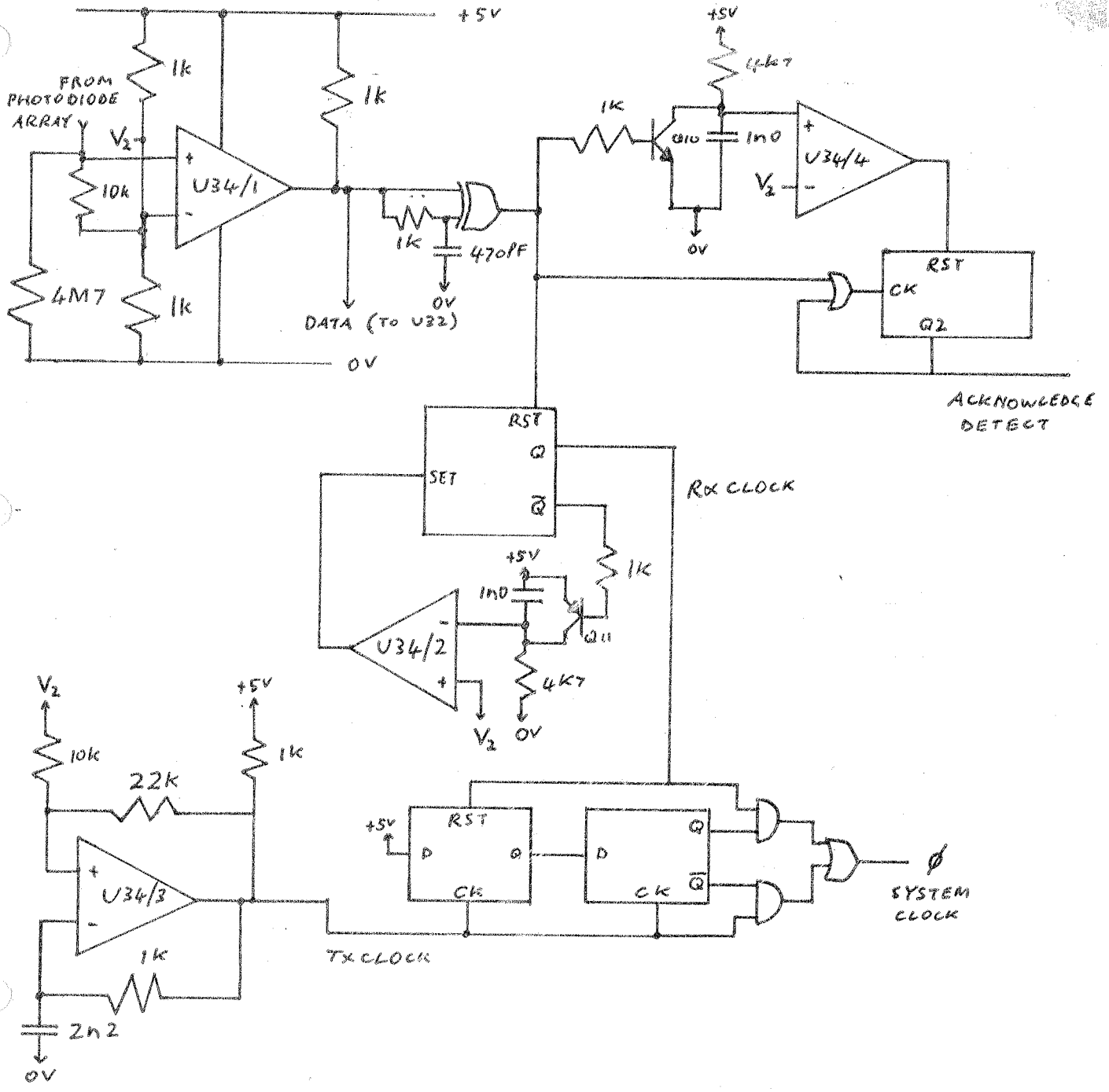


FIG9 CLOCK REGENERATION

is high, the counter counts, but as soon as the monostable output goes low, the counter is reset. The acknowledge detect signal comes from the third bit of the counter, so after 4 cycles of 0 or 1 without a break an acknowledge is deemed to have ocurred.

The operations of all the functional units are controlled by the control state machine (see Fig. 10). It has outputs controlling the shift register, the word count register, the handshaking operations, the data encoder chain and a number of other synchronising and housekeeping functions. It consists of two 2048 by 8 ROMS (2716), with 16 states (taking up four address lines and four data lines for the next-state control) and has 12 control outputs and 7 sense inputs, making it a 16 bit by 2048 machine. The state machine starts off by initialising the finder state machine so it can start looking for incoming signals (state 0), and then waits for the presence of either a transmit request from the external data source (the data flow processing element) or a "found" signal from the finder state machine (state 1). If a transmit request is detected first, then the state machine goes to the start of the transmit sequence (state 5). It loads the shift register (which is acting as the input register at this stage) with the first word from the processing element, which contains the destination address and the number of words to be sent (see Fig dd). The addressing flip-flops of the finder state machine and the word count register are then loaded with the appropriate bits from the shift register (state 5). In this transmitting mode the finder state machine is disabled and its output address is

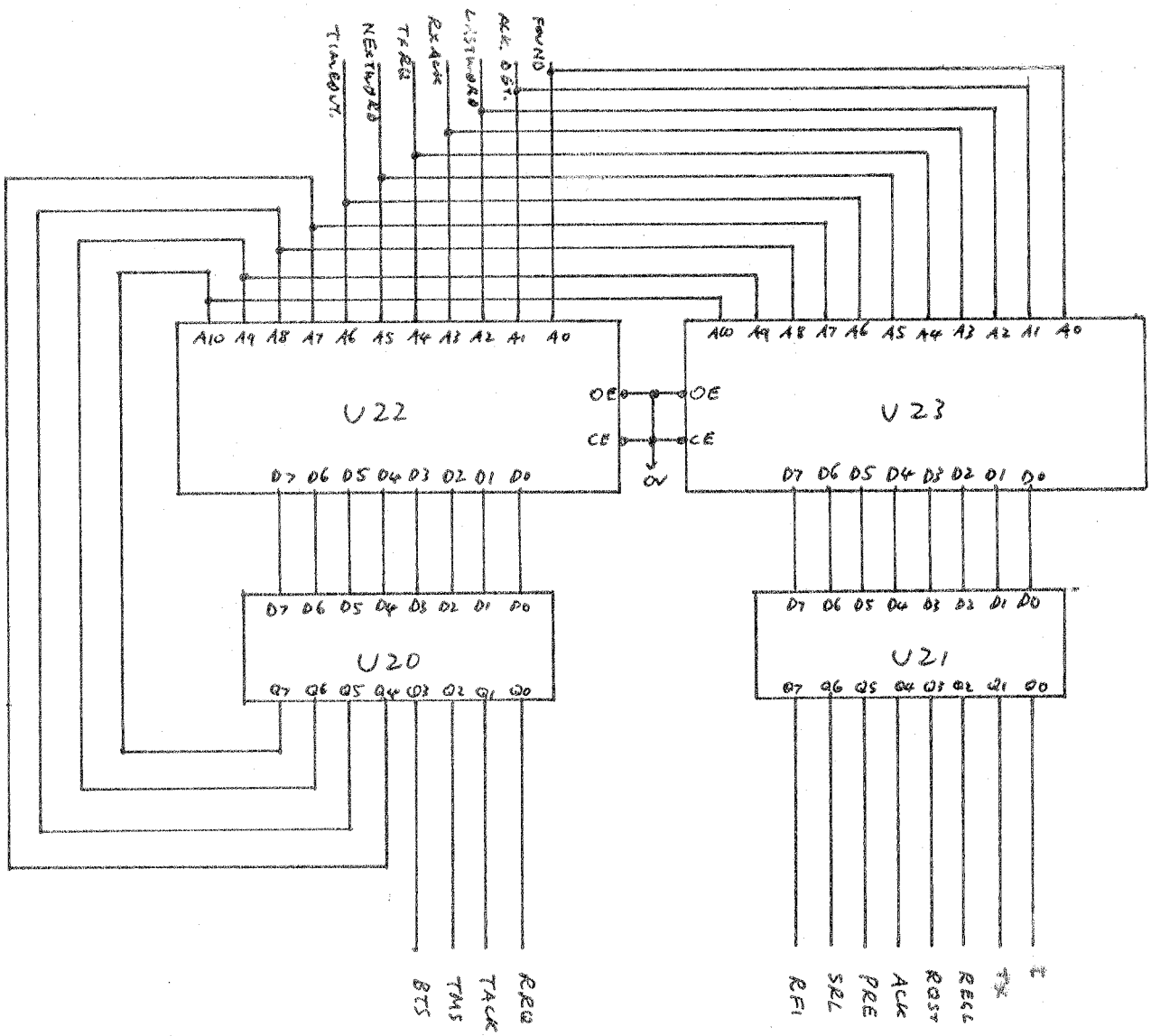


FIG 10 CONTROL STATE MACHINE

therefore fixed so only the photodiode to which an acknowledge is expecting to be sent is enabled. The LED accessed by the address register is then turned on to signify a request to the destination board, and an acknowledge is awaited (state 6). At the same time the timer is started which produces a timeout signal after 16 cycles. If after 16 cycles an acknowledge has not occurred, the sending board enters a backoff state (state 7), which uses the random number generator and the timer to produce a random delay of 1 to 15 cycles. After this delay, the sending board sends a request again, or, if "found" is active, enters the receive state. This scheme provides handling of contentions, ie when two processors are trying to send to each other at the same time. If an acknowledge is detected within the 16 cycles, the preamble is sent (state 8), which synchronises the receiver with the transmitter, and then the data is sent (states 9 and 10). The bits of each word are counted by the bit counter, which sets the next-word flip-flop and decrements the word count register when it reaches 0. The next-word flip-flop indicates to the state machine that the next word is to be loaded and a handshake operation performed (state 9). This sequence is repeated until the word count register reaches a value of one, after which the state machine returns to waiting in state 1.

The receive sequence is complementary to the sending sequence. When a "found" is detected, an acknowledge is sent (state 2) and the state machine waits for the bit counter to count down to zero and set the next-word flip-flop to initiate a handshake. The bit counter is initially disabled until the end

of preamble is detected, at which time it starts counting. When it reaches zero the output register is loaded, the word count register is decremented and the next-word flip-flop is set. As with the transmitting case, the next-word flip-flop indicates the need to perform a handshake operation (state 3) and the cycle is continued until the word count register reaches a value of zero.

IV. RESULTS

Simulation of the System on RMIT Cyber.

A simulation of the system was performed on the RMIT Cyber using a PASCAL program written explicitly for the purpose. This program is available from the Cyber or from Dr. Egan, as well as a set of supporting programs. The main program is called OPSIM and it requires the files ROMFILE and FIRELST to run. These files contain, respectively, the contents of the ROM, and a list describing which processing elements will request transmission ("fire") at what times, and what data will be sent. ROMFILE is generated by a program called PALROM which converts a state machine description into ROM data. The state machine description is contained in a file called PALPROG. The program OPSIM performs a detailed simulation of the design, simulating all functional blocks and the state machine. The simulator proved to be very effective in debugging the design, both the hardware design and the state machine software. It also was able to provide interesting statistical data describing the performance of the system under various loads. The program

FIREGEN was used to produce lists of firingtimes in a random manner. The output of OPSIM is in two files, RUNLIST and STATLST, the first containing detailed information about the boards sending and receiving (ie the state they are in and the contents of the registers), and the second containing summary information - how many packets were sent by each unit and how many cycles it took.

Prototype.

At the date of writing, the prototype has been fully designed and two boards have been constructed. Extensive optical tests have been performed and the signal levels obtained with the prototpye optical arrangement are quite adequate, but the response speed is limited to about 2us. Reliable signal detection was observed for a 250kHz modulation, but above 300kHz, the performance was poor. The prototype runs at 250kbits/sec.

Taking into account the delays introduced by the request, acknowledge and preamble before any data is sent, this speed is substantially lower than is desirable. The communications system would be the "bottleneck" in the data flow computer, as with most other systems. If the data rate could be improved to at least 10Mbits/sec, the design may be a feasible system, but as it stands it is too slow.

The main aim of this project was to study the requirements and produce a prototype that satisfies the geometric and optical requirements, and not necessarily produce

a useable working model. The low data rate achieved does not, therefore, mean that the project was a failure but it does highlight the amount of work needed to produce a workable system.

Monolithic Fabrication of LED and Photodiode Arrays.

The physical size of the prototype could be reduced fairly substantially by replacing the discrete logic forming the search FSM and the ROMs forming the control FSM with PALs (Programmable Array Logic devices). The design could be expanded to cater for 64 units in an 8x8 array, but beyond this the concept starts to become unworkable. For a start, each of the 64 units requires 63 LEDs and 63 photodiodes, making a total of 4032 of each. The photodiodes used in the prototype cost about $20 in 100+ quantities, making the cost for the photodiodes alone over $80,000. This problem was thought to be solvable by fabricating integrated photodiode and LED arrays on silicon wafers. For example, a 64x64 array would easily fit on a standard 2-inch wafer, and costs would be quite low. However, upon examining the optical arrangement needed to support this, it was soon found that there were severe difficulties. If the spacing of the integrated photodiodes was 0.5mm, making the array 32x32mm, the lens focal length 5cm, and the spacing of the boards 20cm, the optical path length would need to be 20m. The system would thus be an array of processors covering an area of 12.8x12.8m, with a mirror the same size suspended 10m above them. The limiting factor is that a lens with f-number of less

than about 1.5 is rather expensive to construct, so the distance from the lens to the array must be at least 1.5 times greater than the diameter of the array (keeping the lens as large as the array to keep light loss to a minimum). The smaller the distance between the elements of the LED and photodiode arrays, the greater the path length has to be to obtain a given deflection. If a wafer with elements 10 um apart was used (instead of 500 um = 0.5 mm), and the focal length was 5 cm as before, the path length required would then be 500 m, a ridiculously large figure implying a building 250 m high. Reducing the distance between boards to only 5 cm (which is the approximate size that is envisaged for the RMIT data flow processors in integrated form) reduces the path length to 62.5 m which is more reasonable but still too large. There is thus a practical limit to the size of the system in array form, imposed by the physical extent of the system in both vertical and horizontal directions. In addition a few other factors must be considered. The (very large) mirror must be solidly mounted so that it does not vibrate or flex, as the alignment is fairly critical for a large arrangement. An optical path length of 20m (as calculated above) is 10 times that of the prototype, giving only 1/100th the power at the receiver unless larger lenses are used, and this in turn limits the proximity of the active devices and the lens. Longer path lengths exacerbate this problem, especially if the light sources are in integrated form, where power dissipation is limited. The integrated photodiodes would probably be simple p-n junctions and would probably be even slower than the prototype. Calculations have not been performed, but by analogy with

observations from the discrete arrangement, it is doubtful that the beams could be focussed finely enough on the receiving array to avoid reception of a signal by more than one photodiode, particularly if 10 um separations are to be used. A large system could not be built with adjustable lens positions as the alignment is much too critical to be "fiddled". The system would have to be built so that all the optics were aligned by the structure, a very difficult proposition indeed. Some of these problems, such as the propogation losses, are overcome when lasers are used instead of LEDs, but then other problems such as alignment may become even more serious. The monolithic approach is suitable for an expansion up to about 64 by 64 elements, but beyond this it also suffers from physical restrictions. Expansion to arbitrarily large scales is not as simple as was hoped.

Large Data Flow Systems.

The use of optical communications structure for large data flow computers requires the use of better optical systems than were used in the prototype. If laser sources deflected by a compact electro-optic device are used, the concept may be very effective. Such a device may be an integrated beam switching system as described before. As described above, the use of free space optical links has physical limitations and does not appear to offer the best solution for communications in an extremely large data-flow system of say 1024 by 1024 processors. The issue of communications in such a processor is still very much an

unsolved problem.

V. CONCLUSIONS

The experimental design outlined here implements the optical communications concept for data flow computers on a prototype basis. It validates the optical array approach and provides the protocol for reliable communications. It satisfies some of the most important requirements for such a communiation system, but does not satisfy speed or cost requirements satisfactorily. The extension of the design to a larger scale was found to be impractical in its present form, but would probably be viable with more advanced optics.

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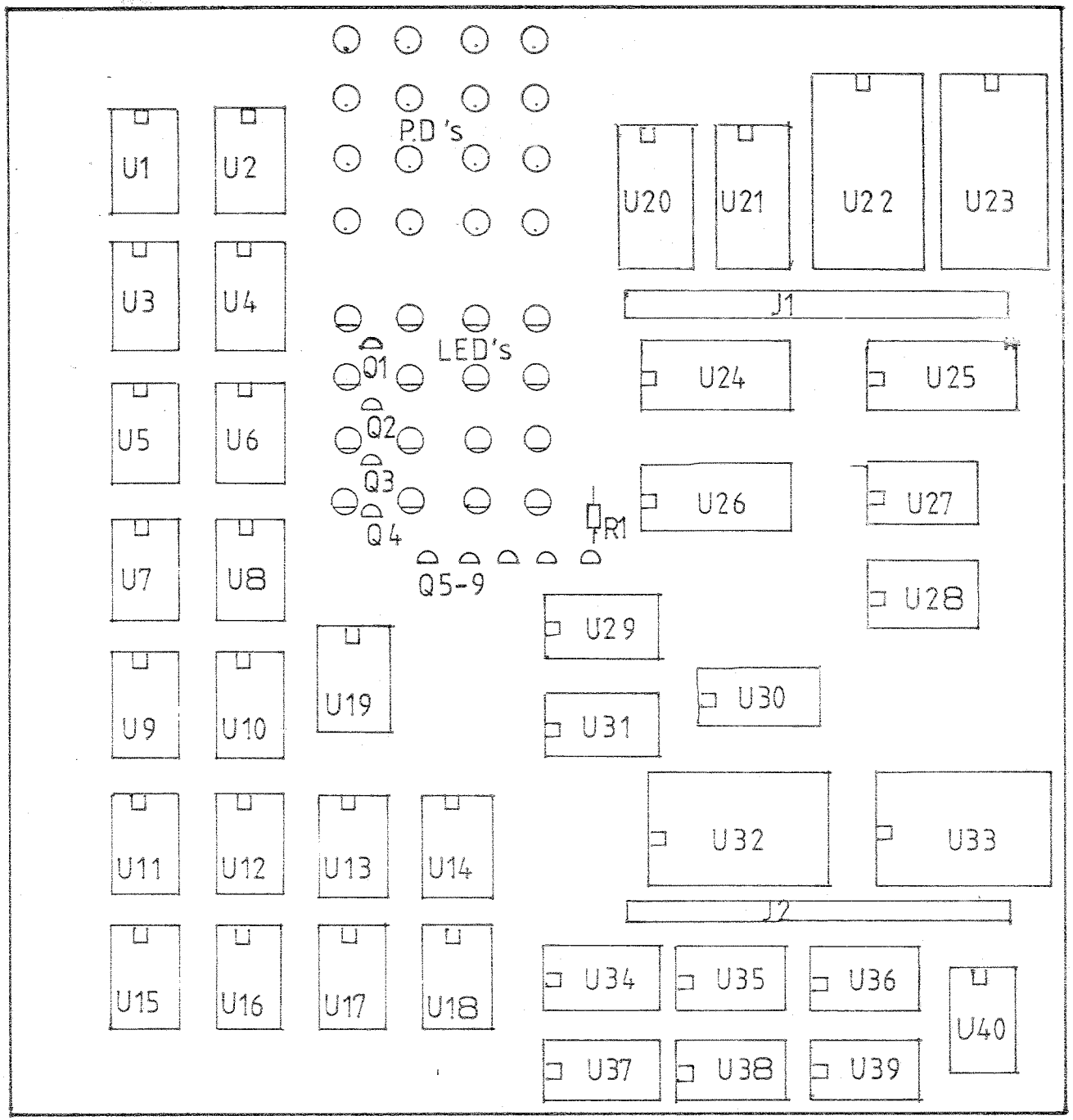
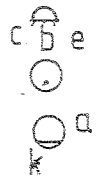
APPENDIX A: PARTS LIST
COMPONENT OVERLAY
P.C.B LAYOUT

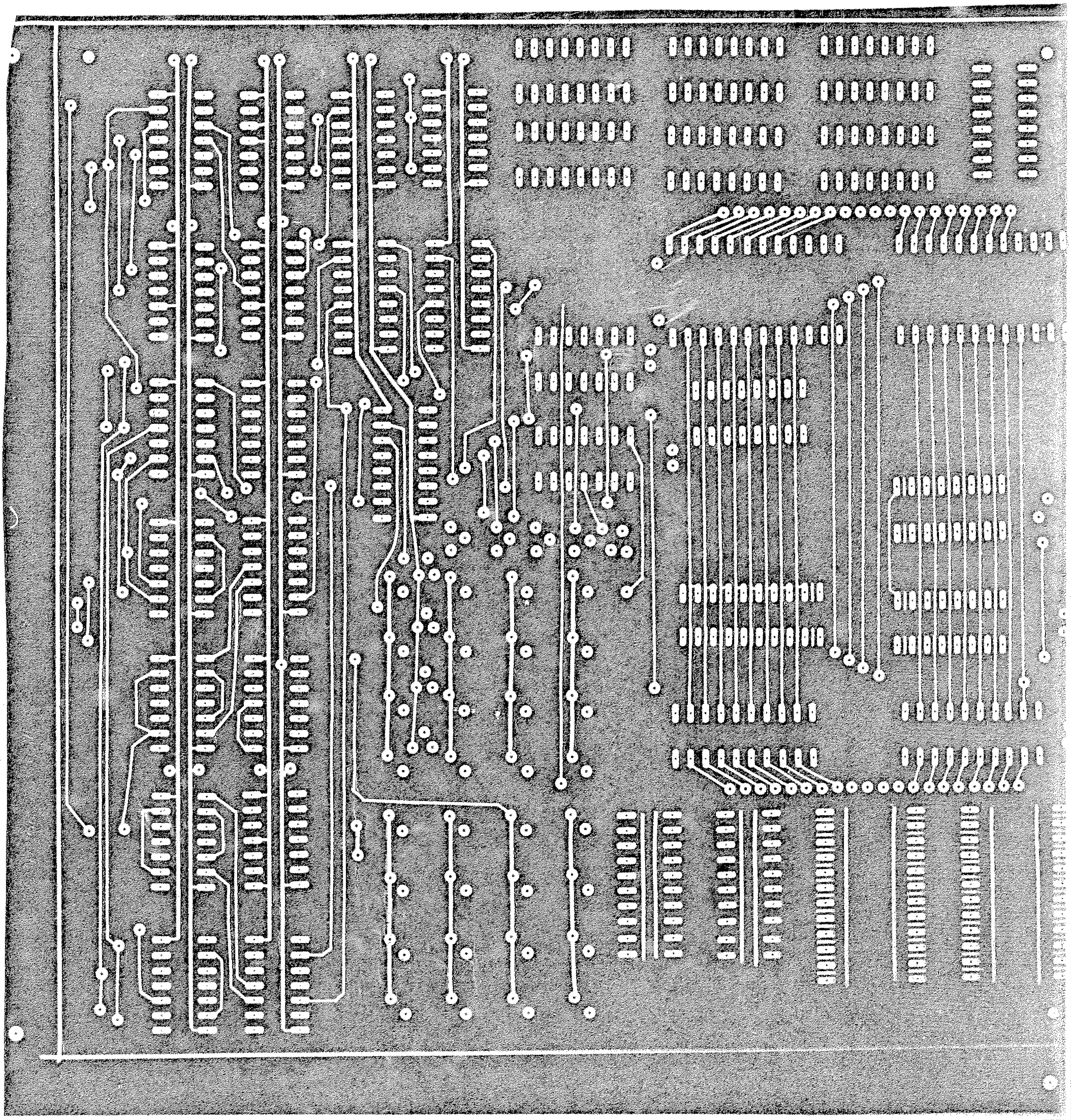
Parts List

U1,3,5,7	4071
U2,8	4081
U4,6	4066
U9	4069
U10,11,12,16,17	4013
U13,14	Not Used
U15,18	4001
U19	4555
U20,21,24,25	74LS574
U22,23	2716
U26	Not Used
U27,28	4516
U29	4011
U30	74C85
U31	4030
U32,33	4034
U34	LM339
U35	4013
U36	74C164
U37,38	4516
U39	4011
U40	Not Used.
Q1-11	BC549
LEDs	HLMP 3750
Photodiodes	HP 5082-4220



COMPONENT
P.C.B LAYOUT





APPENDIX B: DATA SHEETS

HEWLETT PACKARD

PIN PHOTODIODES

5082-4200 SERIES

TECHNICAL DATA JANUARY 198

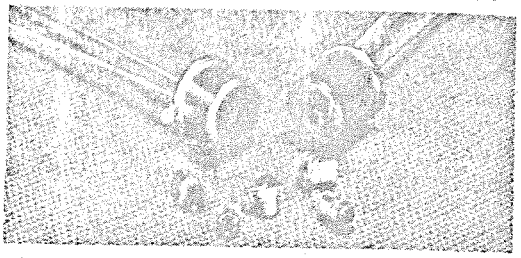
Features

- HIGH SENSITIVITY (NEP<-100 dBm)
- WIDE DYNAMIC RANGE (1% LINEARITY OVER 100 dB)
- BROAD SPECTRAL RESPONSE
- HIGH SPEED (T_r, T_f<1ns)
- STABILITY SUITABLE FOR PHOTOMETRY/ RADIOMETRY
- HIGH RELIABILITY
- FLOATING, SHIELDED CONSTRUCTION
- LOW CAPACITANCE
- LOW NOISE

Active area: 1mm Diam — 5082-4207, 5082-4203, 5082-4204 — TALL SIZE (TO-18)

0.5mm Diam — 5082-4220 — Short (TO-46)

0.25mm Magnified 2.5x — 5082-4205 — Subminiature



Description

The HP silicon planar PIN photodiodes are ultra-fast light detectors for visible and near infrared radiation. Their response to blue and violet is unusually good for low dark current silicon photodiodes.

These devices are suitable for applications such as high speed tachometry, optical distance measurement, star tracking, densitometry, radiometry, and fiber-optic termination.

The speed of response of these detectors is less than one nanosecond. Laser pulses shorter than 0.1 nanosecond may be observed. The frequency response extends from dc to 1 GHz.

The low dark current of these planar diodes enables detection of very low light levels. The quantum detection efficiency is constant over ten decades of light intensity, providing a wide dynamic range.

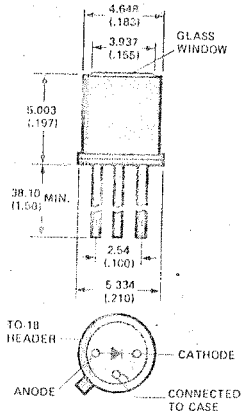
The 5082-4203, -4204, and -4207 are packaged on a standard TO-18 header with a flat glass window cap. For versatility of circuit connection, they are electrically insulated from the header. The light sensitive area of the 5082-4203 and -4204 is 0.508mm (0.020 inch) in diameter and is located 1.905mm (0.075 inch) behind the window. The light sensitive area of the 5082-4207 is 1.016mm (0.040 inch) in diameter and is also located 1.905mm (0.075 inch) behind the window.

The 5082-4205 is in a low capacitance Kovar and ceramic package of very small dimensions, with a hemispherical glass lens.

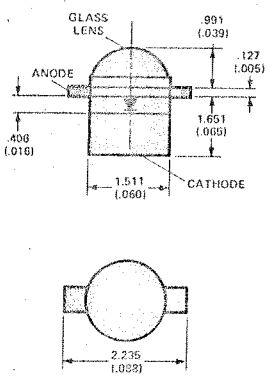
The 5082-4220 is packaged on a TO-46 header with the 0.508mm(0.020 inch) diameter sensitive area located 2.540mm (0.100 inch) behind a flat glass window.

Package Dimensions

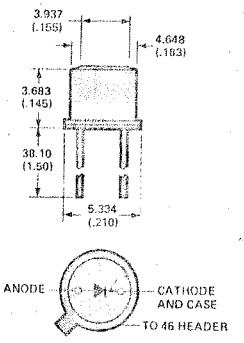
DIMENSIONS IN MILLIMETRES (INCHES)



-4203, -4204, -4207



-4205



-4220

Absolute Maximum Ratings Operating and Storage Temperature -55° to 125°C

Parameter	-4203	-4204	-4205	-4207	-4220	Units
Peak Power Dissipation 1	100	100	50	100	100	mW
Steady Reverse Voltage 3	50	20	50	20	50	volts

Electrical/Optical Characteristics at T_A=25°C

Symbol	Description	-4203 Min.	-4203 Typ.	-4203 Max.	-4204 Min.	-4204 Typ.	-4204 Max.	-4205 Min.	-4205 Typ.	-4205 Max.	-4207 Min.	-4207 Typ.	-4207 Max.	-4220 Min.	-4220 Typ.	-4220 Max.	Units
R_ϕ or R_ϕ * A	Axial Incidence Response at 770nm [4]		1.0			1.0			1.5*			4.0			1.0		$\frac{mA}{mW/cm^2}$
A	Active Area [4]		2 x 10^{-3}			2 x 10^{-3}			3 x 10^{-3}*			8 x 10^{-3}			2 x 10^{-3}		cm^2
R_ϕ	Flux Responsivity 770 nm [5] (Fig. 1, 3)		.4			.5			.5			.5			.5		$\frac{\mu A}{\mu W}$
I_D	Dark Current [9] (Fig. 4)			2.0			0.6			.15			2.5			0.8	nA
NEP	Noise Equivalent Power 7 (Fig. 8)			5.1 x 10^{-14}			2.8 x 10^{-14}			1.4 x 10^{-14}			5.7 x 10^{-14}			8.1 x 10^{-14}	$\frac{W}{\sqrt{Hz}}$
D*	Detectivity 8	3.7 x 10^{11}			1.6 x 10^{12}			4.8 x * 10^{12}			1.6 x 10^{12}			6.6 x 10^{11}			$\frac{cm\sqrt{Hz}}{W}$
C_J	Junction Capacitance [10] (Fig. 6)		1.5			2.0			0.7			5.6			2.0		pF
C_p	Package Capacitance 10		2			2						2					pF
t_r, t_f	Zero Bias Speed (Rise, Fall Time) 11		300			300			300			300			300		ns
t_r, t_f	Rev.-Bias Speed (Rise, Fall Time) 12			1			1			1			1			1	ns
R_S	Series Resistance			50			50			50			50			50	Ω

*see Note 4.

NOTES:

1. Peak Pulse Power

When exposing the diode to high level incidance the following photocurrent limits must be observed:

$$I_{p\ (avg\ MAX.)} < \frac{P_{MAX} - P_\phi}{E_c}$$; and in addition:

$$I_{p(PEAK)} < \frac{1000\ A}{t\ (\mu sec)} \text{ or } <500mA \text{ or } < \frac{I_{p\ (avg\ MAX.)}}{f \times t}$$

whichever of the above three conditions is least.

I_p - photocurrent (A) f - pulse repetion rate (MHz)
E_c - supply voltage (V) P_ϕ - power input via photon flux
t - pulse duration (μs) P_{MAX} - max dissipation (W)

Power dissipation limits apply to the sum of both the optical power input to the device and the electrical power input from flow of photocurrent when reverse voltage is applied.

2. Exceeding the Peak Reverse Voltage will cause permanent damage to the diode. Forward current is harmless to the diode, within the power dissipation limit. For optimum performance, the diode should be reversed biased with E_c between 5 and 20 volts.
3. Exceeding the Steady Reverse Voltage may impair the low-noise properties of the photodiodes, an effect which is noticeable only if operation is diode-noise limited (see Figure 8).
4. The 5082-4205 has a lens with approximately 2.5x magnification; the actual junction area is 0.5 x 10^{-3} cm^2, corresponding to a diameter of 0.25mm (.010"). Specification includes lens effect.
5. At any particular wavelength and for the flux in a small spot falling entirely within the active area, responsivity is the ratio of incremental photodiode current to the incremental flux producing it. It is related to quantum efficiency, η_q in electrons per photon by:

$$R_\phi = \eta_q \left(\frac{\lambda}{1240}\right)$$

where λ is the wavelength in nanometers. Thus, at 770nm, a responsivity of 0.5 A/W corresponds to a quantum efficiency of 0.81 (or 81%) electrons per photon.

6. At -10V for the 5082-4204, -4205, and -4207; at -25V for the 5082-4203 and -4220.
7. For (λ, f, Δf) = (770nm, 100Hz, 6Hz) where f is the frequency for a spot noise measurement and Δf is the noise bandwidth, NEP is the optical flux required for unity signal/noise ratio normalized for bandwidth. Thus:

$$NEP = \frac{I_N/\sqrt{\Delta f}}{R_\phi}$$ where $I_N/\sqrt{\Delta f}$ is the bandwidth -- normalized noise current computed from the shot noise formula:

$I_N/\sqrt{\Delta f} = \sqrt{2qI_D} = 17.9 \times 10^{-15} \sqrt{I_D}$ (A/$\sqrt{Hz}$) where I_D is in nA.

$$D^* = \frac{\sqrt{A}}{NEP}\left(\frac{cm\sqrt{Hz}}{W}\right)$$ for A in cm^2,

8. Detectivity, D*is the active-area-normalized signal to noise ratio. It is computed for (λ, f, Δf) = (770nm, 100Hz, 6Hz).
9. At -10V for 5082-4204, -4205, -4207, -4220; at -25V for 5082-4203.
10. Between diode cathode lead and case -- does not apply to 5082-4205, -4220.
11. With 50Ω load.
12. With 50Ω load and -20V bias.

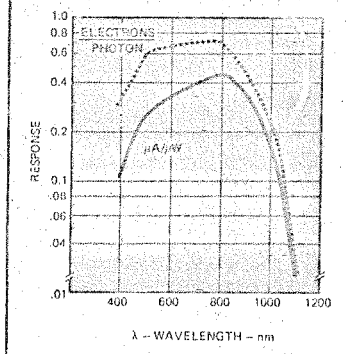


Figure 1. Spectral Response.

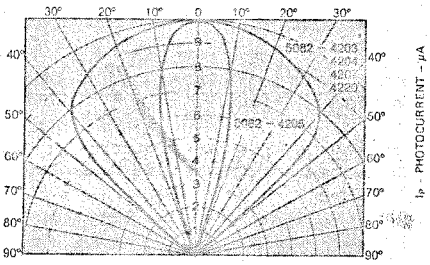


Figure 2. Relative Directional Sensitivity of the PIN Photodiodes.

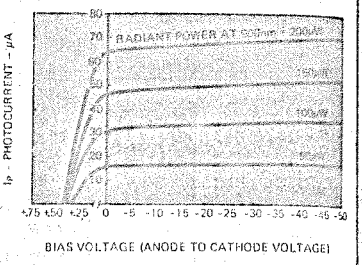


Figure 3. Typical Output Characteristics at λ = 900nm.

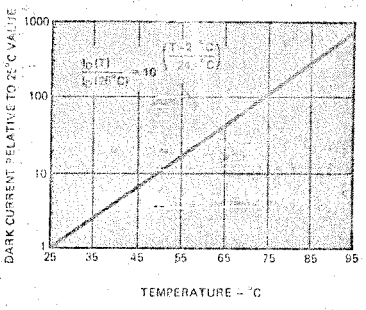


Figure 4. Dark Current at –10V Bias vs. Temperature.

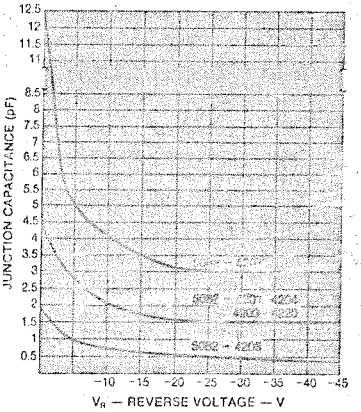


Figure 5. Typical Capacitance Variation With Applied Voltage.

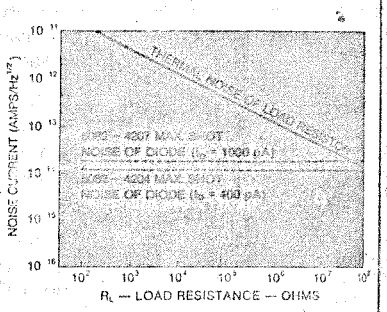


Figure 6. Noise vs. Load Resistance.

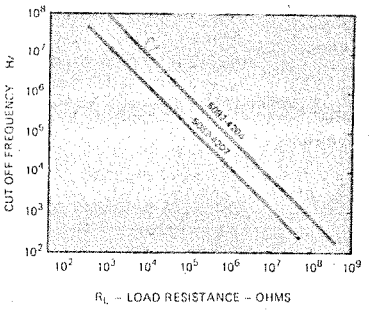


Figure 7. Photodiode Cut-Off Frequency vs. Load Resistance (C = 2pF).

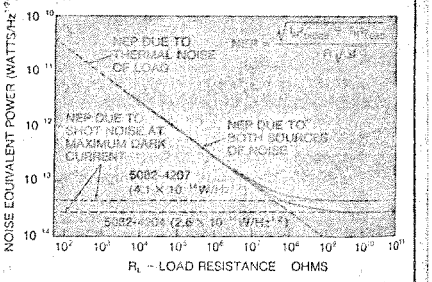


Figure 8. Noise Equivalent Power vs. Load Resistance.

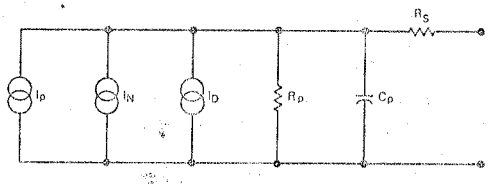


Figure 9. Photodiode Equivalent Circuit.

Ip=Signal current ≈ 0.5μA/μW x flux input at 770 nm
I_N = Shot noise current
<1.2 x 10–14 amps/Hz1/2(5082-4204)
<4 x 10–14 amps/Hz1/2(5082-4207)
I_D = Dark current
<600 x 10–12 amps at –10 V dc (5082-4204)
<2500 x 10–12 amps at –10 V dc (5082-4207)
R_P = 1011Ω
R_S = <50Ω

Application Information

NOISE FREE PROPERTIES

The noise current of the PIN diodes is negligible. This is a direct result of the exceptionally low leakage current, in accordance with the shot noise formula $I_N = (2qI_R\Delta f)^{1/2}$. Since the leakage current does not exceed 600 picoamps for the 5082-4204 at a reverse bias of 10 volts, shot noise current is less than 1.4×10^{-14} amp $Hz^{-1/2}$ at this voltage.

Excess noise is also very low, appearing only at frequencies below 10 Hz, and varying approximately as 1/f. When the output of the diode is observed in a load, thermal noise of the load resistance (R_L) is 1.28×10^{-10} $(R_L)^{-1/2} \times (\Delta f)^{1/2}$ at 25°C, and far exceeds the diode shot noise for load resistance less than 100 megohms (see Figure 6). Thus in high frequency operation where low values of load resistance are required for high cut-off frequency, all PIN photodiodes contribute virtually no noise to the system (see Figures 6 and 7).

HIGH SPEED PROPERTIES

Ultra-fast operation is possible because the HP PIN photodiodes are capable of a response time less than one nanosecond. A significant advantage of this device is that the speed of response is exhibited at relatively low reverse bias (−10 to −20 volts).

OFF-AXIS INCIDANCE RESPONSE

Response of the photodiodes to a uniform field of radiant incidance E_e, parallel to the polar axis is given by $I = (RA) \times E_e$ for 770nm. The response from a field not parallel to the axis can be found by multiplying (RA) by a normalizing factor obtained from the radiation pattern at the angle of operation. For example, the multiplying factor for the 5082-4207 with incidance E_e at an angle of 40° from the polar axis is 0.8. If $E_e = 1mW/cm^2$, then $I_p = k \times (RA) \times E_e$; $I_p = 0.8 \times 4.0 \times 1 = 3.2$ μamps.

SPECTRAL RESPONSE

To obtain the response at a wavelength other than 770nm, the relative spectral response must be considered. Referring to the spectral response curve, Figure 1, obtain response, X, at the wavelength desired. Then the ratio of the response at the desired wavelength to response at 770nm is given by:

$$\text{RATIO} = \frac{X}{0.5}$$

Multiplying this ratio by the incidance response at 770nm gives the incidance response at the desired wavelength.

ULTRAVIOLET RESPONSE

Under reverse bias, a region around the outside edge of the nominal active area becomes responsive. The width of this annular ring is approximately 25μm (0.001 inch) at −20V, and expands with higher reverse voltage. Responsivity in this edge region is higher than in the interior, particularly at shorter wavelengths; at 400nm the interior, responsivity is 0.1 A/W while edge responsivity is 0.35 A/W. At wavelengths shorter than 400nm, attenuation by the glass window affects response adversely. Speed of response for edge incidance is t_r, $t_f \approx 300$ns.

5082-4205 MOUNTING RECOMMENDATIONS

a. The 5082-4205 is intended to be soldered to a printed circuit board having a thickness of from 0.51 to 1.52mm (0.02 to 0.06 inch).
b. Soldering temperature should be controlled so that at no time does the case temperature approach 280°C. The lowest solder melting point in the device is 280°C (gold-tin eutectic). If this temperature is approached, the solder will soften, and the lens may fall off. Lead-tin solder is recommended for mounting the package, and should be applied with a small soldering iron, for the shortest possible time, to avoid the temperature approaching 280°C.
c. Contact to the lens end should be made by soldering to one or both of the tabs provided. Care should be exercised to prevent solder from coming in contact with the lens.
d. If printed circuit board mounting is not convenient, wire leads may be soldering or welded to the devices using the precautions noted above.

LINEAR OPERATION

Having an equivalent circuit as shown in Figure 9, operation of the photodiode is most linear when operated with a current amplifier as shown in Figure 10.

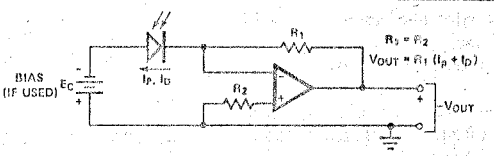


Figure 10. Linear Operation.

Lowest noise is obtained with $E_c = 0$, but higher speed and wider dynamic range are obtained if $5 < E_c < 20$ volts. The amplifier should have as high an input resistance as possible to permit high loop gain. If the photodiode is reversed, bias should also be reversed.

LOGARITHMIC OPERATION

If the photodiode is operated at zero bias with a very high impedance amplifier, the output voltage will be:

$$V_{OUT} = \left(1 + \frac{R_2}{R_1}\right) \cdot \frac{kT}{q} \cdot \ell n \left(1 + \frac{I_P}{I_S}\right)$$

where $I_S = I_F \left(e^{\frac{qV}{kT}} - 1\right)^{-1}$ at $0 < I_F < 0.1$mA

using a circuit as shown in Figure 11.

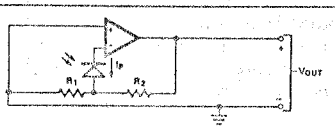


Figure 11. Logarithmic Operation.

Output voltage, V_{OUT}, is positive as the photocurrent, I_P, flows back through the photodiode making the anode positive.

National Semiconductor

CD4001BM/CD4001BC Quad 2-Input NOR Buffered B Series Gate
CD4011BM/CD4011BC Quad 2-Input NAND Buffered B Series Gate

General Description

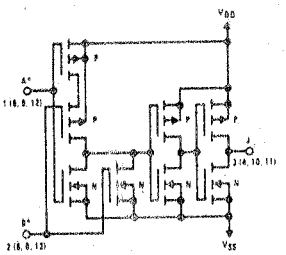
These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 5V—10V—15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1μA at 15V over full temperature range

Schematic and Connection Diagrams



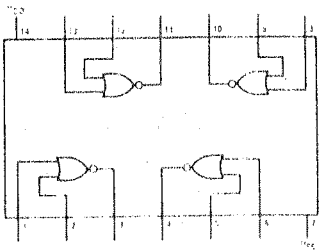
1/4 of device shown

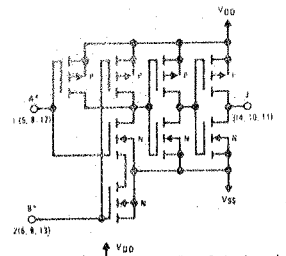
$J = \overline{A + B}$

Logical "1" = High
Logical "0" = Low

*All inputs protected by standard CMOS protection circuit

CD4001BC/CD4001BM
Dual-In-Line and Flat Package





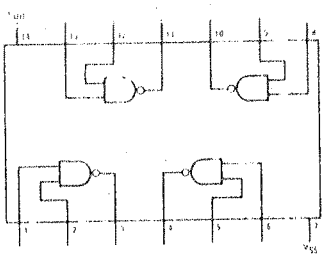
1/4 of device shown

$J = \overline{A \cdot B}$

Logical "1" = High
Logical "0" = Low

*All inputs protected by standard CMOS protection circuit.

CD4011BC/CD4011BM
Dual-In-Line and Flat Package



Absolute Maximum Ra

at Any Pin
Dissipation
Temperature
Temperature (Soldering, 10 seconds

DC Electrical Characte

PARAMETER	
Quiescent Device Current	V_D
	V_D
	V_D
Low Level Output Voltage	V_D
	V_D
	V_D
High Level Output Voltage	V_D
	V_D
	V_D
Low Level Input Voltage	V_D
	V_D
	V_D
High Level Input Voltage	V_D
	V_D
	V_D
Low Level Output Current	V_D
	V_D
	V_D
High Level Output Current	V_D
	V_D
	V_D
Input Current	V_D
	V_D

1. "Absolute Maximum Ratings" ar
ature Range" they are not meant
conditions for actual device operat
2. All voltages measured with respect

ered

fere

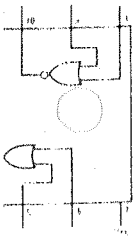
fan out of 2 driving 74L
or 1 driving 74LS

ratings

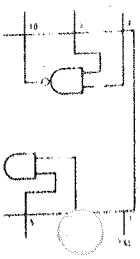
teristics

at 15V over full tempera

1001BM
lat Package



4011BM
lat Package



Solute Maximum Ratings (Notes 1 and 2)

at Any Pin	−0.5V to V_{DD} + 0.5V
Dissipation	500 mW
Range	−0.5 V_{DC} to +18 V_{DC}
Temperature	−65°C to +150°C
Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

Operating V_{DD} Range	3 V_{DC} to 15 V_{DC}
Operating Temperature Range	
CD4001BM, CD4011BM	−55°C to +125°C
CD4001BC, CD4011BC	−40°C to +85°C

Electrical Characteristics CD4001BM, CD4011BM (Note 2)

PARAMETER	CONDITIONS	−55°C		+25°C			+125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
Quiescent Device Current	V_{DD} = 5V		0.25		0.004	0.25		7.5	μA
	V_{DD} = 10V		0.50		0.005	0.50		15	μA
	V_{DD} = 15V		1.0		0.006	1.0		30	μA
Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1μA		0.05		0	0.05		0.05	V
	V_{DD} = 10V, $\lvert I_O \rvert$ < 1μA		0.05		0	0.05		0.05	V
	V_{DD} = 15V, $\lvert I_O \rvert$ < 1μA		0.05		0	0.05		0.05	V
High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1μA	4.95		4.95	5		4.95		V
	V_{DD} = 10V, $\lvert I_O \rvert$ < 1μA	9.95		9.95	10		9.95		V
	V_{DD} = 15V, $\lvert I_O \rvert$ < 1μA	14.95		14.95	15		14.95		V
Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V		1.5		2	1.5		1.5	V
	V_{DD} = 10V, V_O = 9.0V		3.0		4	3.0		3.0	V
	V_{DD} = 15V, V_O = 13.5V		4.0		6	4.0		4.0	V
High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V	3.5		3.5	3		3.5		V
	V_{DD} = 10V, V_O = 1.0V	7.0		7.0	6		7.0		V
	V_{DD} = 15V, V_O = 1.5V	11.0		11.0	9		11.0		V
Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
	V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
	V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
	V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" conditions for actual device operation.

All voltages measured with respect to V_{SS} unless otherwise specified.

DC Electrical Characteristics CD4001BC, CD4011BC (Note 2)

PARAMETER		CONDITIONS	−40°C MIN	−40°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.004	1		7.5
		V_{DD} = 10V		2		0.005	2		15
		V_{DD} = 15V		4		0.006	4		30
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95	
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95	
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$	14.95		14.95	15		14.95	
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V		1.5		2	1.5		1.5
		V_{DD} = 10V, V_O = 9.0V		3.0		4	3.0		3.0
		V_{DD} = 15V, V_O = 13.5V		4.0		6	4.0		4.0
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V	3.5		3.5	3		3.5	
		V_{DD} = 10V, V_O = 1.0V	7.0		7.0	6		7.0	
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0	9		11.0	
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36	
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9	
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4	
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36	
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9	
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4	
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0

AC Electrical Characteristics CD4001BC, CD4001BM

T_A = 25°C, Input t_r; t_f = 20 ns. C_L = 50 pF, R_L = 200k. Typical temperature coefficient is 0.3%/°C.

PARAMETER		CONDITIONS	TYP	MAX	Units
t_{PHL}	Propagation Delay Time, High-to-Low Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	V_{DD} = 5V	110	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

Electrical Characte

T_A = 25°C, Input t_r; t_f = 20 ns.

PARAMETE	
t_{PHL}	Propagation Delay
t_{PLH}	Propagation Delay
t_{THL}, t_{TLH}	Transition Time
C_{IN}	Average Input Ca
C_{PD}	Power Dissipation

ypical Performance C

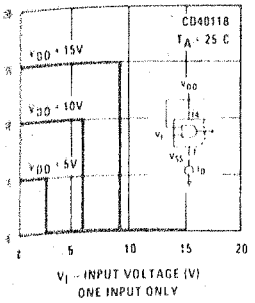


FIGURE 1. Typical Transfer Characteristics

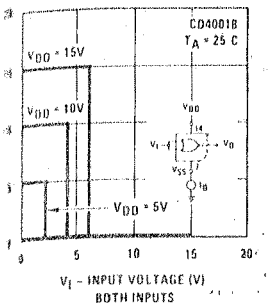


FIGURE 4. Typical Transfer Characteristics

Electrical Characteristics CD4011BC, CD4011BM

T_A = 25°C, Input t_r; t_f = 20 ns, C_L = 50 pF, R_L = 200k. Typical Temperature Coefficient is 0.3%/°C.

	PARAMETER	CONDITIONS	TYP	MAX	UNITS
t_{PHL}	Propagation Delay, High-to-Low Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{PLH}	Propagation Delay, Low-to-High Level	V_{DD} = 5V	85	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

Typical Performance Characteristics

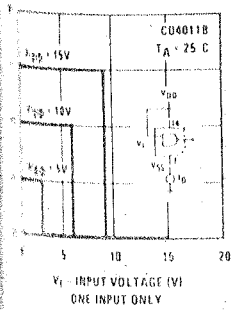


FIGURE 1. Typical Transfer Characteristics

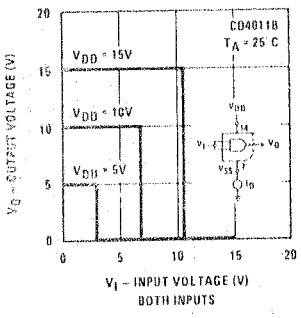


FIGURE 2. Typical Transfer Characteristics

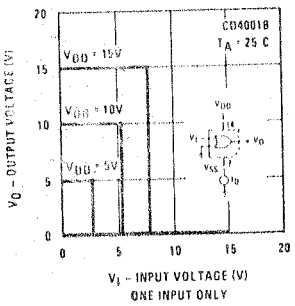


FIGURE 3. Typical Transfer Characteristics

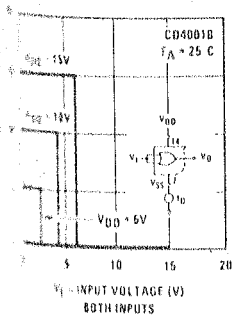


FIGURE 4. Typical Transfer Characteristics

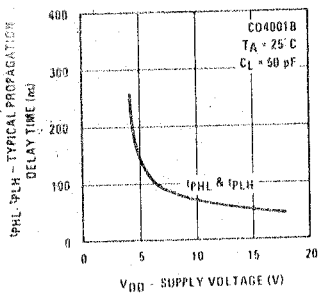


FIGURE 5

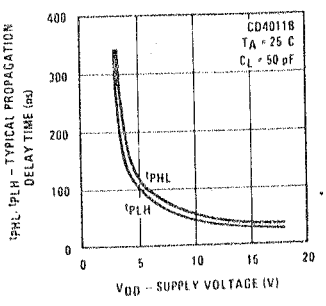


FIGURE 6

Typical Performance Characteristics (Cont'd.)

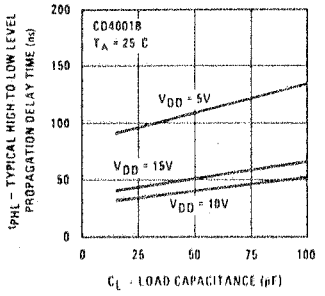


FIGURE 7

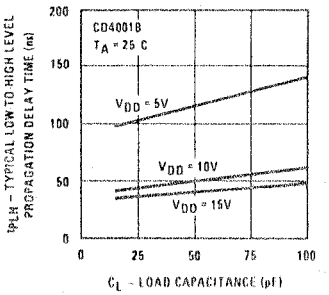


FIGURE 8

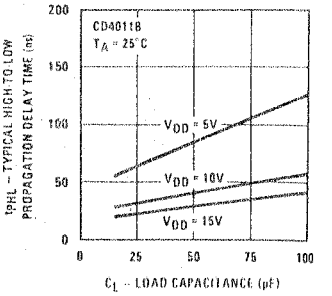


FIGURE 9

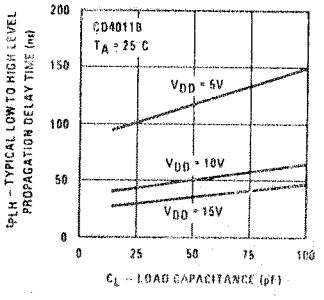


FIGURE 10

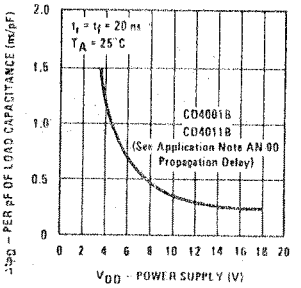


FIGURE 11

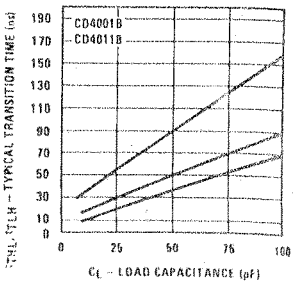


FIGURE 12

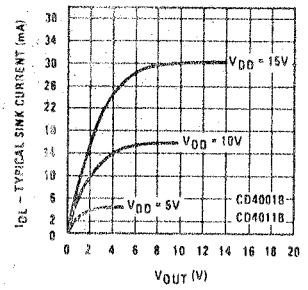


FIGURE 13

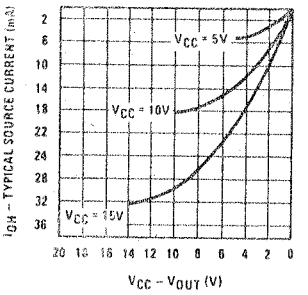


FIGURE 14

Nation Semic

CD4002M/CI
CD4012M/CI

General Descrip

These NOR and NAND ga
tary MOS (CMOS) inte
P-channel enhancement
symmetrical circuit with
to the supply voltage. This
over a wide supply volta
than that caused by leaka
static conditions. All inpu
discharge and latching c

Connection Diagr

National Semiconductor

CD4013BM/CD4013BC Dual D Flip-Flop

General Description

The CD4013B dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

Features

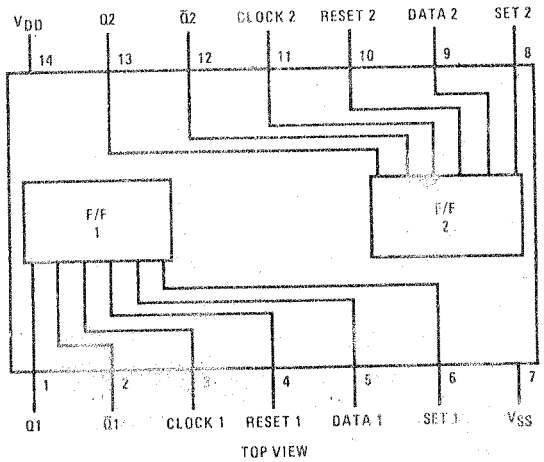
Wide supply voltage range	3.0 V to 15 V
High noise immunity	0.45 V_{DD} (typ.)
Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

Connection Diagram

Dual-In-Line and Flat Package



TOP VIEW

Truth Table

CL†	D	R	S	Q	$\overline{Q}$
⌐↑	0	0	0	0	1
⌐↑	1	0	0	1	0
↓⌐	x	0	0	Q	$\overline{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

No change
† = Level change
x = Don't care case

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	+3 to +15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4013BM	−55°C to +125°C
CD4013BC	−40°C to +85°C

DC Electrical Characteristics 4013BM (Note 2)

PARAMETER		CONDITIONS	−55°C MIN	−55°C MAX	25°C MIN	25°C TYP	25°C MAX	125°C MIN	125°C MAX	UNITS
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		30	μA
		V_{DD} = 10V		2.0			2.0		60	μA
		V_{DD} = 15V		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics 4013BC (Note 2)

PARAMETER		CONDITIONS	−40°C MIN	−40°C MAX	25°C MIN	25°C TYP	25°C MAX	85°C MIN	85°C MAX	UNITS
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4.0			4.0		30	μA
		V_{DD} = 10V		8.0			8.0		60	μA
		V_{DD} = 15V		16.0			16.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V

DC Electrical Char

PARAMETER	
V_{IH}	High Level Input Voltage
I_{OL}	Low Level Output Current
I_{OH}	High Level Output Curren
I_{IN}	Input Current

Note 1: "Absolute Maximum R
that the devices should be opera
conditions for actual device opera
Note 2: V_{SS} = 0V unless otherw

AC Electrical Cha

PARAMETER	
CLOCK OPERATION	
t_{PHL}, or t_{PLH}	Propagation Delay T
t_{THL}, or t_{TLH}	Transition Time
t_{WL}, or t_{WH}	Minimum Clock Puls
t_{RCL}, t_{FCL}	Maximum Clock Ris
t_{SU}	Minimum Set-Up T
f_{CL}	Maximum Clock Fr
SET AND RESET OPERATION	
$t_{PHL(R)}$, $t_{PLH(S)}$	Propagation Delay T
$t_{WH(R)}$, $t_{WH(S)}$	Minimum Set and R Pulse Width
C_{IN}	Average Input Capa

Conditions

+3 to +15 V_{DC}
0 to V_{DD} V_{DC}

−55°C to +125°C
−40°C to +85°C

DC Electrical Characteristics (Cont'd.) CD4013BC (Note 2)

PARAMETER		CONDITIONS	−40°C MIN	−40°C MAX	25°C MIN	25°C TYP	25°C MAX	85°C MIN	85°C MAX	UNITS
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

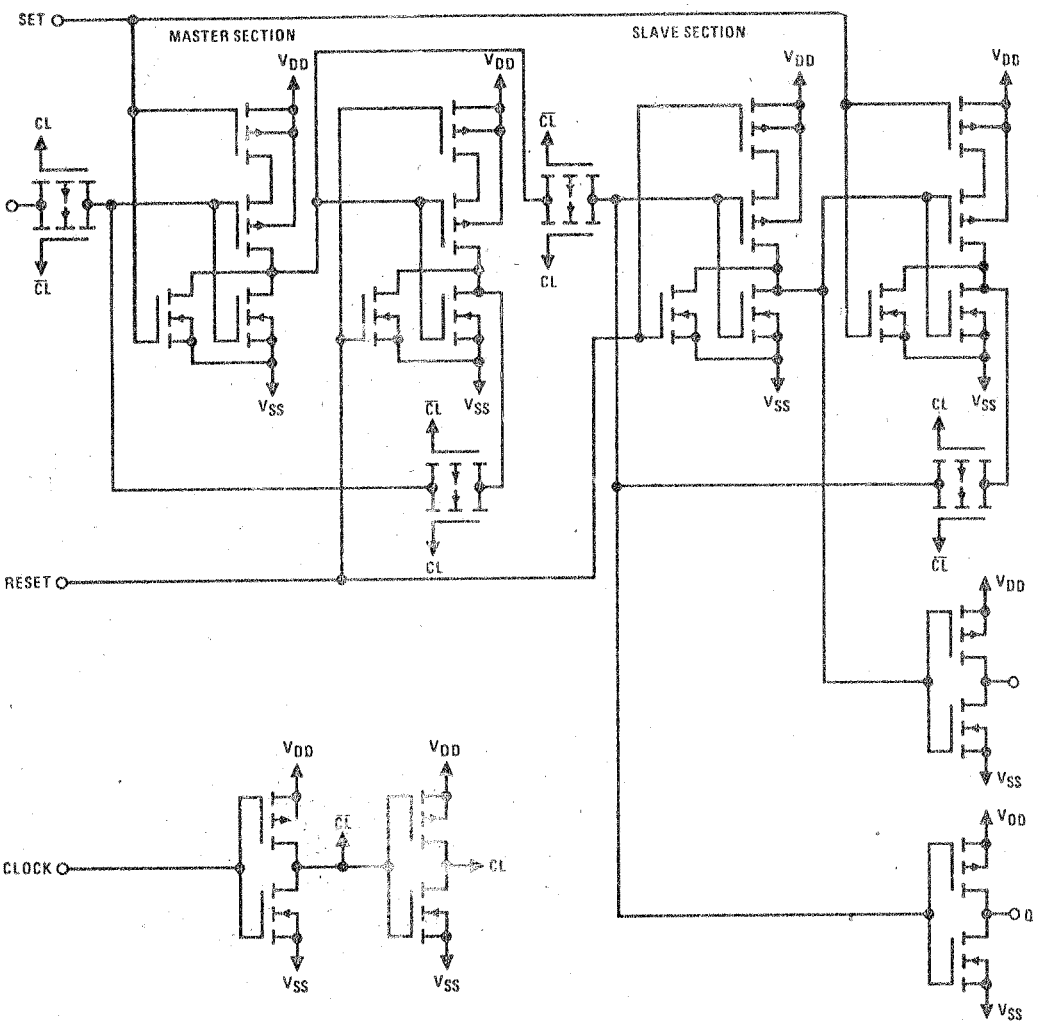
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

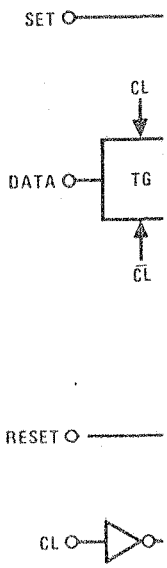
AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, R_L = 200 k, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK OPERATION						
t_{PHL}, or t_{PLH}	Propagation Delay Time	V_{DD} = 5V		200	350	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		65	120	ns
t_{THL}, or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, or t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		32	65	ns
t_{RCL}, t_{FCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			10	μs
		V_{DD} = 15V			5	μs
t_{SU}	Minimum Set-Up Time	V_{DD} = 5V		20	40	ns
		V_{DD} = 10V		15	30	ns
		V_{DD} = 15V		12	25	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	2.5	5		MHz
		V_{DD} = 10V	6.2	12.5		MHz
		V_{DD} = 15V	7.6	15.5		MHz
SET AND RESET OPERATION						
$t_{PHL(R)}$, $t_{PLH(S)}$	Propagation Delay Time	V_{DD} = 5V		150	300	ns
		V_{DD} = 10V		65	130	ns
		V_{DD} = 15V		45	90	ns
$t_{WH(R)}$, $t_{WH(S)}$	Minimum Set and Reset Pulse Width	V_{DD} = 5V		90	180	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		25	50	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF

Schematic Diagram

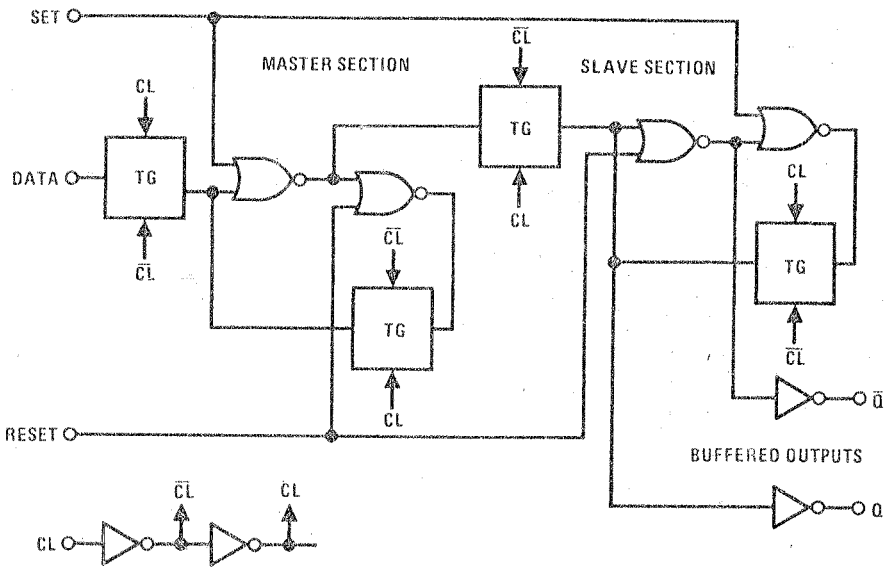


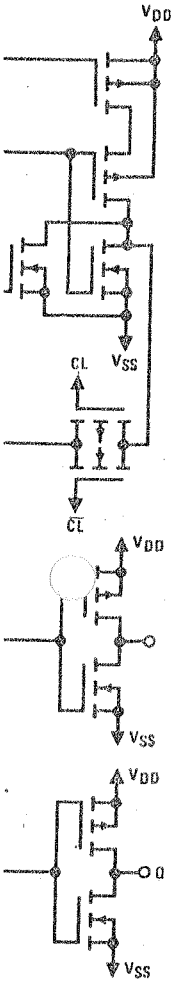
Logic Diagram



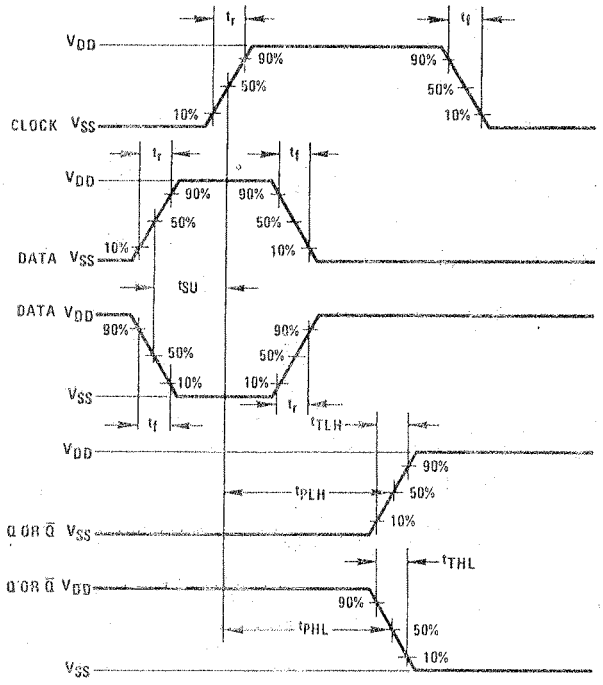
Switching Time Wave

Logic Diagram





Switching Time Waveforms



National Semiconductor

CD4030M/CD4030C Quad EXCLUSIVE-OR Gate

General Description

The EXCLUSIVE-OR gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

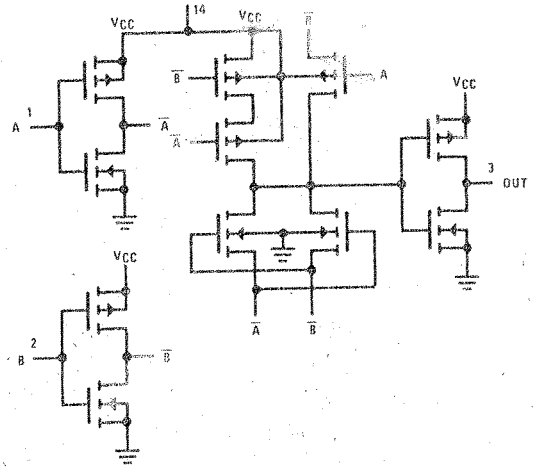
Features

- Wide supply voltage range — 3.0V to 15V
- Low power — 100nW (typ.)
- Medium speed operation — $t_{PHL} = t_{PLH} = 40$ns (typ.) at $C_L = 15$pF, 10V supply
- High noise immunity — 0.45 V_{CC} (typ.)

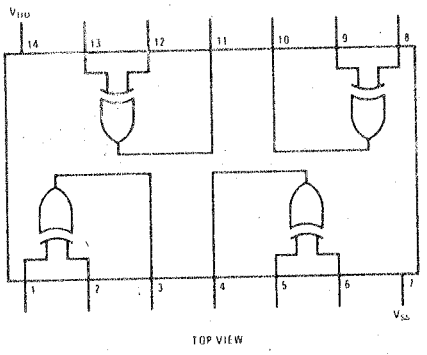
Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

Schematic Diagram



Connection Diagram



TOP VIEW

Absolute Maxin

Voltage at Any Pin (N
Operating Temperatu
CD4030M
CD4030C
Storage Temperature
Package Dissipation
Operating V_{DD} Range
Lead Temperature (So

DC Electrical Ch

PARAMETER	
Quiescent Device Current (I_L)	V V
Quiescent Device Dissipation Package (P_D)	V V
Output Voltage Low Level (V_{OL})	V V
Output Voltage High Level (V_{OH})	V V
Noise Immunity (All Inputs) (V_{NL})	V V
Noise Immunity (All Inputs)(V_{NH})	V V
Output Drive Current N-Channel (I_DN)	V V
Output Drive Current P-Channel (I_DP)	V V
Input Current (I_I)	V

DC Electrical Cha

PARAMETER	
Quiescent Device Current (I_L)	V_{DD} V_{DD}
Quiescent Device Dissipation Package (P_D)	V_{DD} V_{DD}
Output Voltage Low Level (V_{OL})	V_{DD} V_{DD}
Output Voltage High Level (V_{OH})	V_{DD} V_{DD}
Noise Immunity (All Inputs)(V_{NL})	V_{DD} V_{DD}
Noise Immunity (All Inputs)(V_{NH})	V_{DD} V_{DD}
Output Drive Current N-Channel (I_DN)	V_{DD} V_{DD}
Output Drive Current P-Channel (I_DP)	V_{DD} V_{DD}
Input Current (I_I)	V_I = (

Note 1: This device should no damage.

Absolute Maximum Ratings

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
CD4030M	−55°C to +125°C
CD4030C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics CD4030M

PARAMETER	CONDITIONS	LIMITS									UNITS
		-55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			0.5		0.005	0.5			30	μA
	V_{DD} = 10V			1.0		0.01	1.0			60	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			2.5		0.025	2.5			150	μW
	V_{DD} = 10V			10		0.1	10			600	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.05		0	0.05			0.05	V
	V_{DD} = 10V			0.05		0	0.05			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.95			4.95	5.0		4.95			V
	V_{DD} = 10V	9.95			9.95	10		9.95			V
Noise Immunity (All Inputs) (V_{NL})	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (All Inputs) (V_{NH})	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V	0.75			0.6	1.2		0.45			mA
	V_{DD} = 10V	1.5			1.2	2.4		0.9			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V	−0.45			−0.3	−0.6		−0.21			mA
	V_{DD} = 10V	−0.95			−0.65	−1.3		−0.45			mA
Input Current (I_I)	V_I = 0V or V_I = V_{DD}					10					pA

DC Electrical Characteristics CD4030C

PARAMETER	CONDITIONS	LIMITS									UNITS
		-40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5.0		0.05	5.0			70	μA
	V_{DD} = 10V			10		0.1	10			140	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			25		0.25	25			350	μW
	V_{DD} = 10V			100		1.0	100			1,400	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.05		0	0.05			0.05	V
	V_{DD} = 10V			0.05		0	0.05			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.95			4.95	5.0		4.95			V
	V_{DD} = 10V	9.95			9.95	10		9.95			V
Noise Immunity (All Inputs) (V_{NL})	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (All Inputs) (V_{NH})	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0	0.35			0.3	1.2		0.25			mA
	V_{DD} = 10V	0.7			0.6	2.4		0.5			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V	−0.21			−0.15	−0.6		−0.12			mA
	V_{DD} = 10V	−0.45			−0.32	−1.3		−0.25			mA
Input Current (I_I)	V_I = 0V or V_I = V_{DD}					10					pA

Note 1: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

AC Electrical Characteristics CD4030M

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	V_{DD} = 5.0V		100	200	ns
	V_{DD} = 10V		40	100	ns
Propagation Delay Time (t_{PLH})	V_{DD} = 5.0V		100	200	ns
	V_{DD} = 10V		40	100	ns
Transition Time High to Low Level (t_{THL})	V_{DD} = 5.0V		70	150	ns
	V_{DD} = 10V		25	75	ns
Transition Time Low to High Level (t_{TLH})	V_{DD} = 5.0V		80	150	ns
	V_{DD} = 10V		30	75	ns
Input Capacitance (C_I)	V_I = 0V or V_I = V_{DD}		5.0		pF

AC Electrical Characteristics CD4030C

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	V_{DD} = 5.0V		100	300	ns
	V_{DD} = 10V		40	150	ns
Propagation Delay Time (t_{PLH})	V_{DD} = 5.0V		100	300	ns
	V_{DD} = 10V		40	150	ns
Transition Time High to Low Level (t_{THL})	V_{DD} = 5.0V		70	300	ns
	V_{DD} = 10V		25	150	ns
Transition Time Low to High Level (t_{TLH})	V_{DD} = 5.0V		80	300	ns
	V_{DD} = 10V		30	150	ns
Input Capacitance (C_I)	V_I = 0V or V_I = V_{DD}		5.0		pF

Truth Table (For One of Four Identical Gates)

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where: "1" = High Level
"0" = Low Level

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CD4031BI

General Des

The CD4031BM/CD
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LATE input (when M
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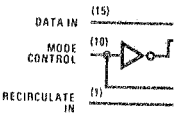

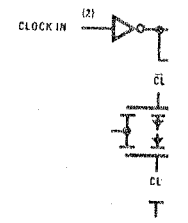

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National Semiconductor

CD4034BM/CD4034BC 8-State TRI-STATE® Bidirectional Parallel/Serial Input/Output Bus Register

General Description

The CD4034BM/CD4034BC is an 8-bit CMOS static shift register with two parallel bidirectional data ports (A and B) which, when combined with serial shifting operations, can be used to (1) bidirectionally transfer parallel data between two buses, (2) convert serial data to parallel form and direct them to either of two buses, (3) store (recirculate) parallel data, or (4) accept parallel data from either of two buses and convert them to serial form. These operations are controlled by five control inputs:

A ENABLE (AE): "A" data port is enabled only when AE is at logical "1". This allows the use of a common bus for multiple packages.

A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B): This input controls the direction of data flow. When at logical "1", data flows from port A to B (A is input, B is output). When at logical "0", the data flow direction is reversed.

ASYNCHRONOUS/SYNCHRONOUS (A/S): When A/S is at logical "0", data transfer occurs at positive transition of the CLOCK. When A/S is at logical "1", data transfer is independent of the CLOCK for parallel operation. In serial mode, A/S input is internally disabled such that operation is always synchronous. (Asynchronous serial operation is not possible.)

PARALLEL/SERIAL (P/S): A logical "1" P/S input allows data transfer into the registers via A or B port (synchronous if A/S = logical "0", asynchronous if A/S = logical "1"). A logical "0" P/S allows serial data to transfer into the register synchronously with the positive transition of the CLOCK, independent of the A/S input.

CLOCK: Single phase, enabled only in synchronous mode. (Either P/S = logical "1" and A/S = logical "0" or P/S = logical "0".

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

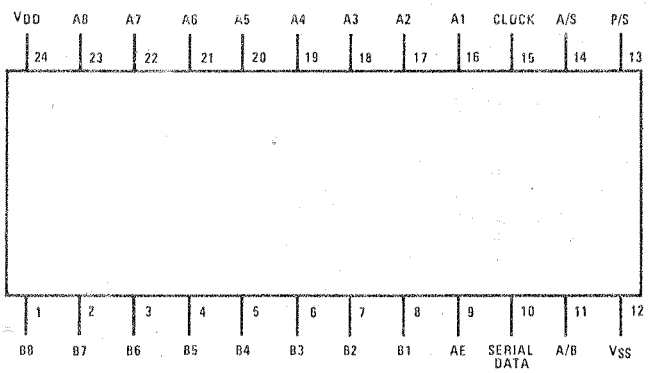
Features

- Wide supply voltage range — 3.0 to 18 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- RCA CD4034B second source

Applications

- Parallel Input/Parallel Output
  Parallel Input/Serial Output
  Serial Input/Parallel Output
  Serial Input/Serial Output register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storge, counting, display)
- Frequency and phase comparator

Connection Diagram



Absolute Maximum Ratings
(Notes 1 and 2)

V_{DD}	DC Supply Voltage	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
V_{IN}	Input Voltage	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
T_S	Storage Temperature Range	$-65°C$ to $+150°C$
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions
(Note 2)

V_{DD}	DC Supply Voltage	$+3\ V_{DC}$ to $+15\ V_{DC}$
V_{IN}	Input Voltage	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
T_A	Operating Temperature Range	
	CD4034BM	$-55°C$ to $+125°C$
	CD4034BC	$-40°C$ to $+85°C$

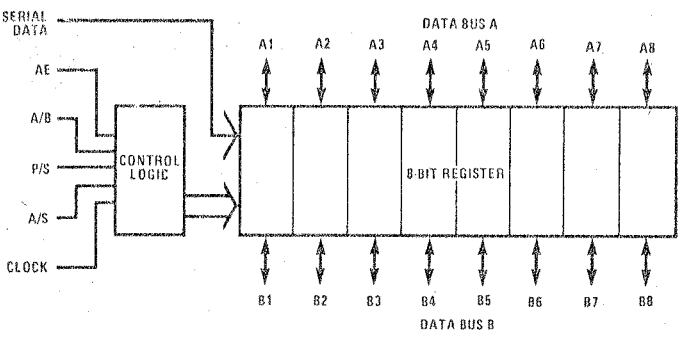
DC Electrical Characteristics CD4034BM (Note 2)

PARAMETER	CONDITIONS	−55°C		+25°C			+125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5\ V$		5			5		150	μA
	$V_{DD} = 10\ V$		10			10		300	μA
	$V_{DD} = 15\ V$		20			20		600	μA
V_{OL} Low Level Output Voltage	$V_{DD} = 5\ V$		0.05			0.05		0.05	V
	$V_{DD} = 10\ V$		0.05			0.05		0.05	V
	$V_{DD} = 15\ V$		0.05			0.05		0.05	V
V_{OH} High Level Output Voltage	$V_{DD} = 5\ V$	4.95		4.95			4.95		V
	$V_{DD} = 10\ V$	9.95		9.95			9.95		V
	$V_{DD} = 15\ V$	14.95		14.95			14.95		V
V_{IL} Low Level Input Voltage	$V_{DD} = 5\ V$, $V_O = 0.5\ V$ or $4.5\ V$		1.5			1.5		1.5	V
	$V_{DD} = 10\ V$, $V_O = 1.0\ V$ or $9.0\ V$		3.0			3.0		3.0	V
	$V_{DD} = 15\ V$, $V_O = 1.5\ V$ or $13.5\ V$		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$V_{DD} = 5\ V$, $V_O = 0.5\ V$ or $4.5\ V$	3.5		3.5			3.5		V
	$V_{DD} = 10\ V$, $V_O = 1.0\ V$ or $9.0\ V$	7.0		7.0			7.0		V
	$V_{DD} = 15\ V$, $V_O = 1.5\ V$ or $13.5\ V$	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	$V_{DD} = 5\ V$, $V_O = 0.4\ V$	0.64		0.51			0.36		mA
	$V_{DD} = 10\ V$, $V_O = 0.5\ V$	1.6		1.3			0.9		mA
	$V_{DD} = 15\ V$, $V_O = 1.5\ V$	4.2		3.4			2.4		mA
I_{OH} High Level Output Current	$V_{DD} = 5\ V$, $V_O = 4.6\ V$	−0.64		−0.51			−0.36		mA
	$V_{DD} = 10\ V$, $V_O = 9.5\ V$	−1.6		−1.3			−0.9		mA
	$V_{DD} = 15\ V$, $V_O = 13.5\ V$	−4.2		−3.4			−2.4		mA
I_{IN} Input Current	$V_{DD} = 15\ V$, $V_{IN} = 0\ V$	−0.1		−0.1	-10^{-5}		−1.0		μA
	$V_{DD} = 15\ V$, $V_{IN} = 15\ V$		0.1		10^{-5}	0.1		1.0	μA
I_{OZ} Tri-State Leakage Current	$V_{DD} = 15\ V$, $V_O = 0\ V$	−0.1		−0.1	-10^{-5}		−1.0		μA
	$V_{DD} = 15\ V$, $V_O = 15\ V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0\ V$ unless otherwise specified.

Logic Diagram



DC Electrical Ch

PARAMETER

I_{DD} Quiescent Device Current

V_{OL} Low Level Output Voltag

V_{OH} High Level Output Voltag

V_{IL} Low Level Input Voltage

V_{IH} High Level Input Voltage

I_{OL} Low Level Output Current

I_{OH} High Level Output Current

I_{IN} Input Current

I_{OZ} Tri-State Leakage Current

AC Electrical Cha

PARAME

t_{PHL}, t_{PLH} Propagation
Synchronous
Data Input, E
Output

t_{PHL}, t_{PLH} Propagation D
A(B) Asynchr
Input, B(A) P

t_{PHZ}, t_{PLZ} Propagation D
or AE to High
Outputs or fr
Impedance St

t_{PZH}, t_{PZL} Propagation D
or AE to Logi
State at A Ou
Logical "1" or
B Outputs

t_{THL}, t_{TLH} Output Transi

f_{CL} Maximum Cloc

t_{WL}, t_{WH} Minimum Cloc

ating Conditions

+3 V_{DC} to +15 V_{DC}
0 V_{DC} to V_{DD} V_{DC}
nge
−55°C to +125°C
−40°C to +85°C

X	+125°C MIN	+125°C MAX	UNITS
		150	μA
		300	μA
		600	μA
5		0.05	V
5		0.05	V
5		0.05	V
	4.95		V
	9.95		V
	14.95		V
		1.5	V
		3.0	V
		4.0	V
	3.5		V
	7.0		V
	11.0		V
	0.36		mA
	0.9		mA
	2.4		mA
	-0.3		mA
	-0.9		mA
	-2.4		mA
	-1.0		μA
		1.0	μA
	-1.0		μA
		1.0	μA

e guaranteed. Except for
s. The table of "Electrical

DC Electrical Characteristics CD4034BC (Note 2)

PARAMETER	CONDITIONS	−40°C MIN	−40°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS
I_{DD} Quiescent Device Current	V_{DD} = 5 V		20			20		150	μA
	V_{DD} = 10 V		40			40		300	μA
	V_{DD} = 15 V		80			80		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5 V		0.05			0.05		0.05	V
	V_{DD} = 10 V		0.05			0.05		0.05	V
	V_{DD} = 15 V		0.05			0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5 V	4.95		4.95			4.95		V
	V_{DD} = 10 V	9.95		9.95			9.95		V
	V_{DD} = 15 V	14.95		14.95			14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V		1.5			1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0			3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V	3.5		3.5			3.5		V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0			7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5 V, V_O = 0.4 V	0.52		0.44			0.36		mA
	V_{DD} = 10 V, V_O = 0.5 V	1.3		1.1			0.9		mA
	V_{DD} = 15 V, V_O = 1.5 V	3.6		3.0			2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5 V, V_O = 4.6 V	−0.52		−0.44			−0.36		mA
	V_{DD} = 10 V, V_O = 9.5 V	−1.3		−1.1			−0.9		mA
	V_{DD} = 15 V, V_O = 13.5 V	−3.6		−3.0			−2.4		mA
I_{IN} Input Current	V_{DD} = 15 V, V_{IN} = 0 V	−0.3		−0.3	-10^{-5}		−1.0		μA
	V_{DD} = 15 V, V_{IN} = 15 V		0.3		10^{-5}	0.3		1.0	μA
I_{OZ} Tri-State Leakage Current	V_{DD} = 15 V, V_O = 0 V	−0.3		−0.3	-10^{-5}		−1.0		μA
	V_{DD} = 15 V, V_O = 15 V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, R_L = 200 k, Input $t_r = t_f$ = 20 ns, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time, A(B) Synchronous Parallel Data or Serial Data Input, B(A) Parallel Data Output	V_{DD} = 5 V		280	700	ns
		V_{DD} = 10 V		120	270	ns
		V_{DD} = 15 V		85	190	ns
t_{PHL}, t_{PLH}	Propagation Delay Time, A(B) A(B) Asynchronous Parallel Data Input, B(A) Parallel Data Output	V_{DD} = 5 V		280	700	ns
		V_{DD} = 10 V		120	270	ns
		V_{DD} = 15 V		85	190	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time from A/B or AE to High Impedance State at A Outputs or from A/B to High Impedance State at B Outputs	V_{DD} = 5 V, R_L = 1.0KΩ		95	220	ns
		V_{DD} = 10 V, R_L = 1.0KΩ		60	130	ns
		V_{DD} = 15 V, R_L = 1.0KΩ		45	100	ns
t_{PZH}, t_{PZL}	Propagation Delay Time from A/B or AE to Logical "1" or Logical "0" State at A Outputs or from A/B to Logical "1" or Logical "0" State at B Outputs	V_{DD} = 5 V, R_L = 1.0KΩ		180	480	ns
		V_{DD} = 10 V, R_L = 1.0KΩ		75	190	ns
		V_{DD} = 15 V, R_L = 1.0KΩ		55	140	ns
t_{THL}, t_{TLH}	Output Transition Time	V_{DD} = 5 V		100	200	ns
		V_{DD} = 10 V		50	100	ns
		V_{DD} = 15 V		40	80	ns
f_{CL}	Maximum Clock Input Frequency	V_{DD} = 5 V	2	4		MHz
		V_{DD} = 10 V	5	10		MHz
		V_{DD} = 15 V	7	14		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5 V		125	250	ns
		V_{DD} = 10 V		50	100	ns
		V_{DD} = 15 V		35	70	ns

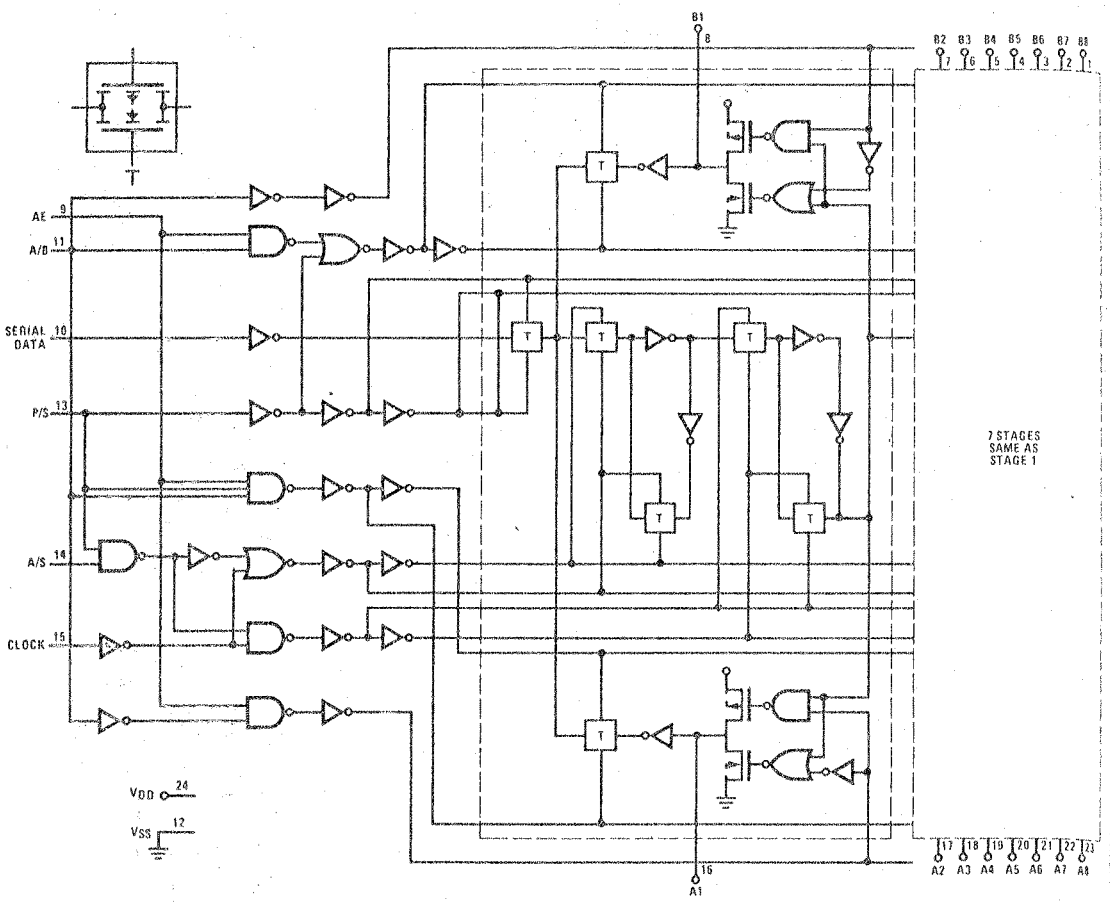
5

AC Electrical Characteristics (Cont'd.)

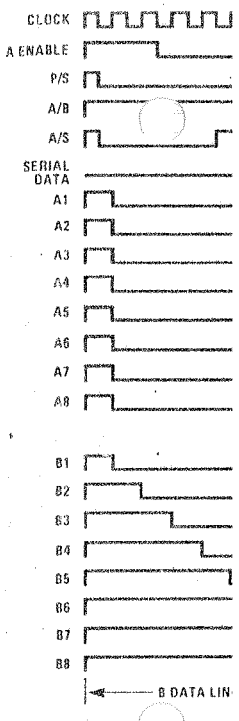
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{RCL}, t_{FCL}	Maximum Clock Rise & Fall Time	V_{DD} = 5 V	15			μs
		V_{DD} = 10 V	15			μs
		V_{DD} = 15 V	15			μs
t_{SU}	Parallel (A or B) and Serial Data Setup Time	V_{DD} = 5 V		25	70	ns
		V_{DD} = 10 V		10	30	ns
		V_{DD} = 15 V		7	20	ns
t_{SU}	Control Inputs AE, A/B, P/S, A/S Setup Time	V_{DD} = 5 V		110	280	ns
		V_{DD} = 10 V		35	100	ns
		V_{DD} = 15 V		20	60	ns
t_{WH}	Minimum High Level AE, A/B, P/S, A/S Pulse Width	V_{DD} = 5 V		160	400	ns
		V_{DD} = 10 V		70	160	ns
		V_{DD} = 15 V		40	90	ns
C_{IN}	Average Input Capacitance	A and B Data I/O and A/B Control Input		7	15	pF
		Any Other Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		155		pF

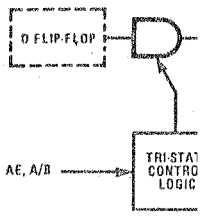
Note 3: C_{PD} determines the no-load power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

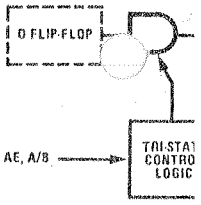
Schematic Diagram



Switching Time \

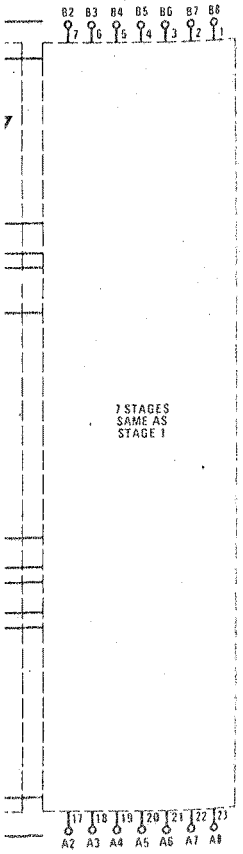




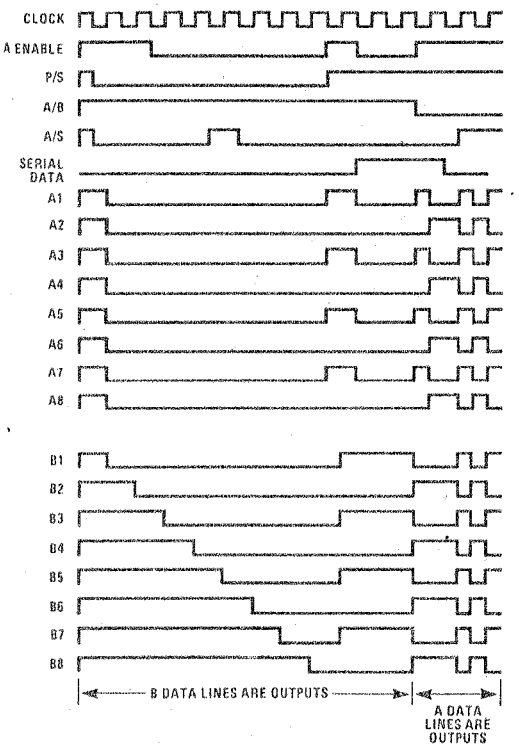


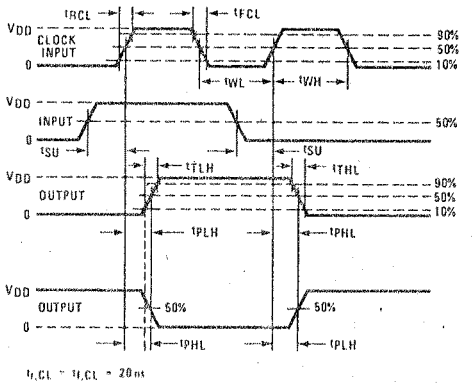
TYP	MAX	UNITS
		μs
		μs
		μs
25	70	ns
10	30	ns
7	20	ns
110	280	ns
35	100	ns
20	60	ns
160	400	ns
70	160	ns
40	90	ns
7	15	pF
5	7.5	pF
155		pF

4C/74C Family Character-



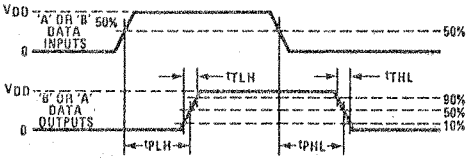
Switching Time Waveforms and Test Circuits



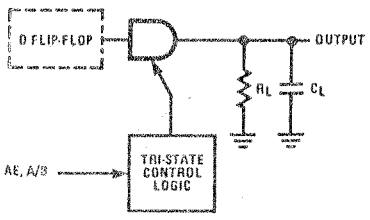


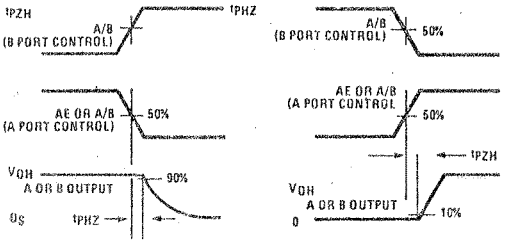
tr,CL = tf,CL = 20 ns

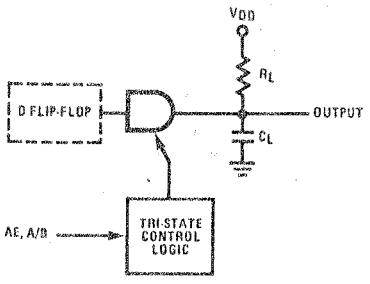
Synchronous Operation

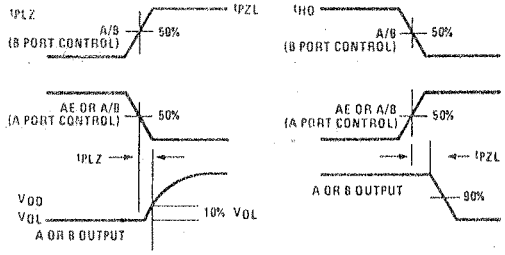


Asynchronous Operation

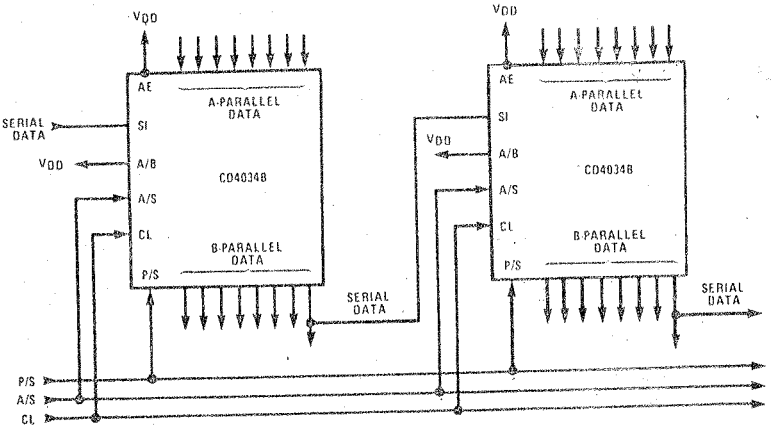




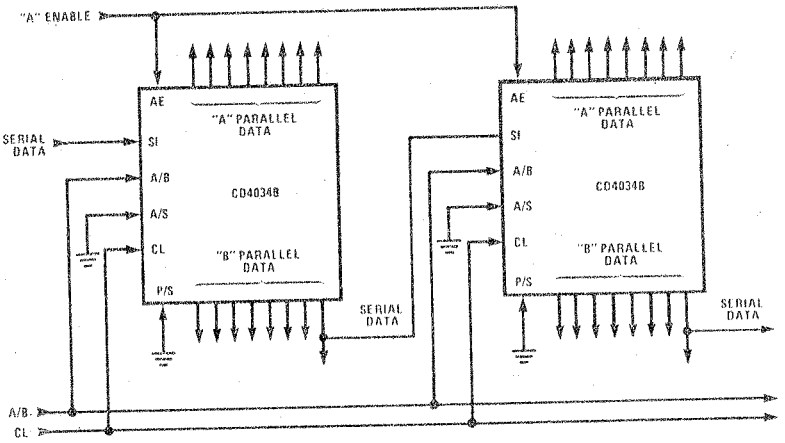




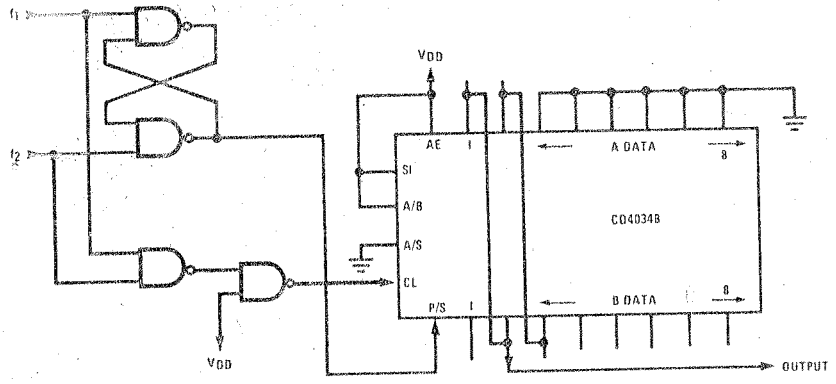
Applications



16-Bit parallel in/parallel out,parallel in/serial out, serial in/parallel out, serial in/serial out register.

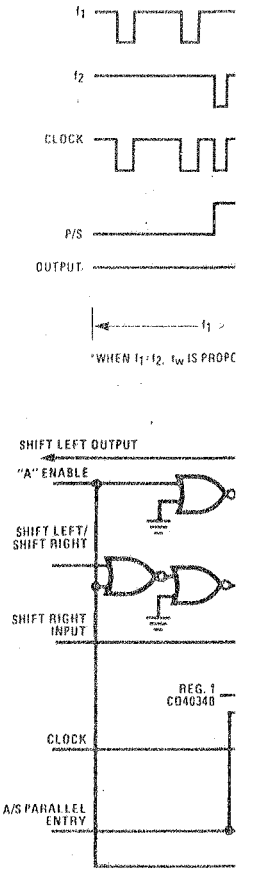


16-Bit serial in/gated parallel out register.



Frequency and Phase Comparator

Applications (Cont'

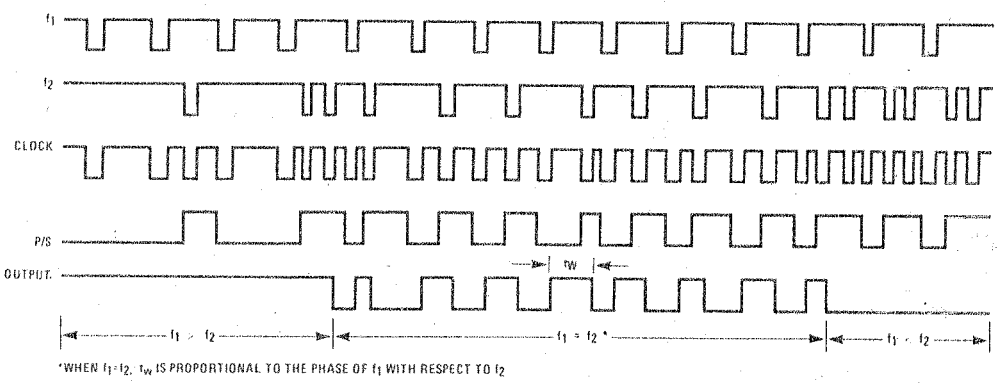


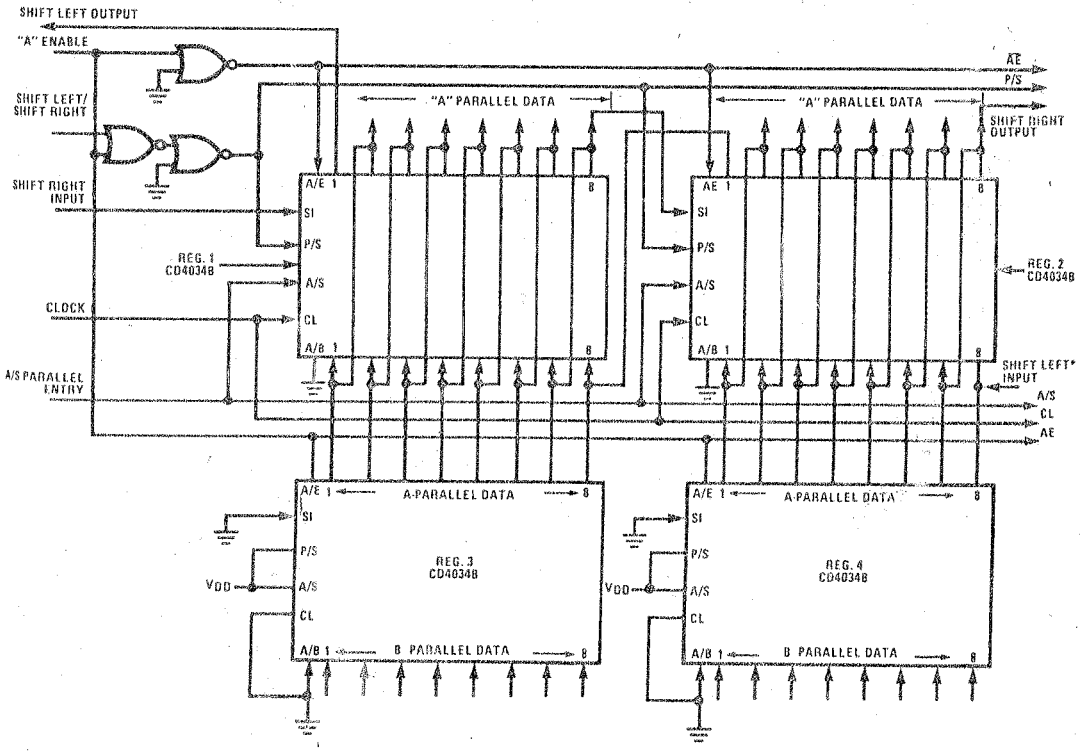
VDD

A "High" ("Low") on allows serial data on th Input) to enter the re of the clock signal. A " disables the "A" paralle and enables the "A" c

*Shift left input must be dis

Applications (Cont'd.)





A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Registers 1 and 2 and enables the "A" data lines on Registers 3 and 4 and allows parallel data into Registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Registers 3 and 4 and associated logic are not required.

*Shift left input must be disabled during parallel entry.

Shift Right/Shift Left with Parallel Inputs

Truth Table

0	1	0	0	Parallel	B Synchronous Parallel data inputs, A Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, synchronous data recirculation.
0	1	1	1	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, asynchronous data recirculation.
1	0	0	X	Serial	Synchronous Serial data input, A-Parallel data output.
1	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
1	1	0	0	Parallel	B Synchronous Parallel data input, A-Parallel data output.
1	1	0	1	Parallel	B Asynchronous Parallel data input, A-Parallel data output.
1	1	1	0	Parallel	A Synchronous Parallel data input, B-Parallel data output.
1	1	1	1	Parallel	A Asynchronous Parallel data input, B Parallel data output.

X = Don't Care

*For synchronous operation (serial mode or when A/S = 0 in parallel mode), outputs change state at positive transition of the clock.

Shift Regis

General Descr

The CD4035B 4-bit p
is a monlithic compl
circuit constructed w
mode transistors. Thi
serial register having
inputs to each stage
via JK logic. Register
serial "D" flip-flop co
the serial mode (para

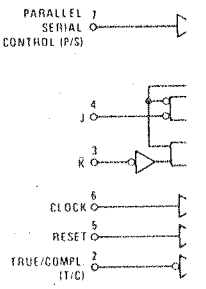
Parallel entry via the
permitted only when

In the parallel or seri
on positive clock tra

When the true/comp
contents of the regis
minals. When the tru
outputs are the comp
The true/complemen
with respect to the c

JK input logic is provi
minimize logic requir
sequence-generation
nected together, the
An asynchronous co

Logic Diagrar



P/S =
T/C =
*TG =

National Semiconductor

CD4069M/CD4069C Inverter Circuits

General Description

The CD4069B consists of six inverter circuits and is manufactured using complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity, and symmetric controlled rise and fall times.

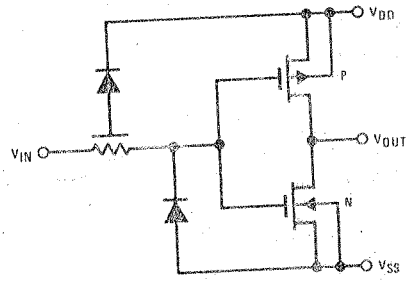
This device is intended for all general purpose inverter applications where the special characteristics of the MM74C901, MM74C903, MM74C907, and CD4049A Hex Inverter/Buffers are not required. In those applications requiring larger noise immunity the MM74C14 or MM74C914 Hex Schmitt Trigger is suggested.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

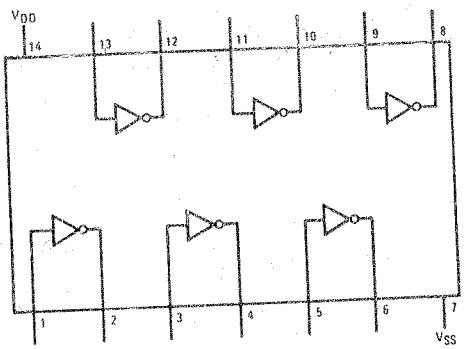
Features

■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} typ.
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Equivalent to MM54C04/MM74C04	

Schematic and Connection Diagrams

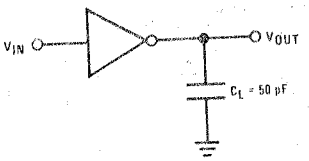


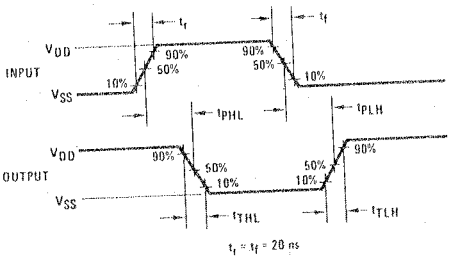
Dual-In-Line Package



TOP VIEW

AC Test Circuits and Switching Time Waveforms





$t_r = t_f = 20$ ns

Absolute Maxim

(Notes 1 and 2)

V_{DD} dc Supply Voltage
V_{IN} Input Voltage
T_S Storage Temperature Range
P_D Package Dissipation
T_L Lead Temperature (Solder

DC Electrical Cha

CD4069M (Note 2)

PARAMETER	
I_{DD}	Quiescent Device Curr
V_{OL}	Low Level Output Vol
V_{OH}	High Level Output Vol
V_{IL}	Low Level Input Volta
V_{IH}	High Level Input Volta
I_{OL}	Low Level Output Curr
I_{OH}	High Level Output Curr
I_{IN}	Input Current

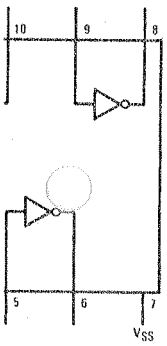
amage due to static dis-
and V_{SS}.

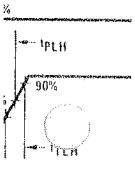
3.0 V to 15 V

0.45 V_{DD} typ.

fan out of 2 driving 74L
or 1 driving 74LS

74C04





Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4069M	−55°C to +125°C
CD4069C	−40°C to +85°C

DC Electrical Characteristics

CD4069M (Note 2)

PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	V_{DD} = 5V		0.25			0.25		7.5	μA
	V_{DD} = 10V		0.5			0.5		15	μA
	V_{DD} = 15V		1.0			1.0		30	μA
V_{OL} Low Level Output Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V		0.05		0	0.05		0.05	V
	V_{DD} = 10V		0.05		0	0.05		0.05	V
	V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V	4.95		4.95	5		4.95		V
	V_{DD} = 10V	9.95		9.95	10		9.95		V
	V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V, V_O = 4.5V		1.5			1.5		1.5	V
	V_{DD} = 10V, V_O = 9V		3.0			3.0		3.0	V
	V_{DD} = 15V, V_O = 13.5V		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V, V_O = 0.5V	3.5		3.5			3.5		V
	V_{DD} = 10V, V_O = 1V	7.0		7.0			7.0		V
	V_{DD} = 15V, V_O = 1.5V	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
	V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
	V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
	V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_N Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

5

DC Electrical Characteristics CD4069C (Note 2)

PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNIT
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	V_{DD} = 5V		1.0			1.0		7.5	μA
	V_{DD} = 10V		2.0			2.0		15	μA
	V_{DD} = 15V		4.0			4.0		30	μA
V_{OL} Low Level Output Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V		0.05		0	0.05		0.05	V
	V_{DD} = 10V		0.05		0	0.05		0.05	V
	V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V	4.95		4.95			4.95		V
	V_{DD} = 10V	9.95		9.95			9.95		V
	V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL} Low Level Input Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V, V_O = 4.5V		1.5			1.5		1.5	V
	V_{DD} = 10V, V_O = 9V		3.0			3.0		3.0	V
	V_{DD} = 15V, V_O = 13.5V		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V, V_O = 0.5V	3.5		3.5			3.5		V
	V_{DD} = 10V, V_O = 1V	7.0		7.0			7.0		V
	V_{DD} = 15V, V_O = 1.5V	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
	V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
	V_{DD} = 15V, V_O = 1.5V	3.6		8.0	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
	V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
	V_{DD} = 15V, V_O = 13.5V	−3.6		−8.0	−8.8		−2.4		mA
I_{IN} Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$, t_r and $t_f \leq 20\,ns$, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL} or t_{PLH}	Propagation Delay Time From Input To Output	V_{DD} = 5V		50	90	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		80	150	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Gate		6	7.5	pF
C_{PD}	Power Dissipation Capacitance	Any Gate (Note 3)		12		pF

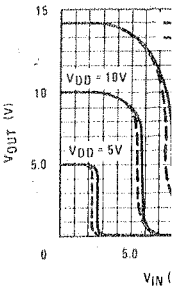
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note—AN-90.

Typical Perf

Gate Transfer C



	85°C		
MAX	MIN	MAX	UNIT
1.0		7.5	μA
2.0		15	μA
4.0		30	μA
0.05		0.05	V
0.05		0.05	V
0.05		0.05	V
	4.95		V
	9.95		V
	14.95		V
1.5		1.5	V
3.0		3.0	V
4.0		4.0	V
	3.5		V
	7.0		V
	11.0		V
	0.36		mA
	0.9		mA
	2.4		mA
	−0.36		mA
	−0.9		mA
	−2.4		mA
−0.30		−1.0	μA
0.30		1.0	μA

≤ 20 ns,

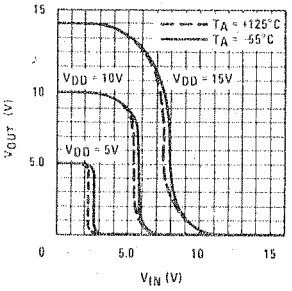
TYP	MAX	UNIT
50	90	ns
30	60	ns
25	50	ns
80	150	ns
50	100	ns
40	80	ns
6	7.5	pF
12		pF

rantee y are not meant to imp
d "Elec Characteristics" provid

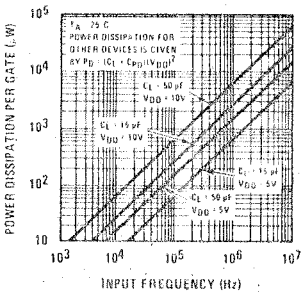
n, see 54C/74C Family Characteristi

Typical Performance Characteristics

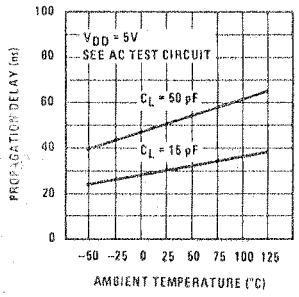
Gate Transfer Characteristics



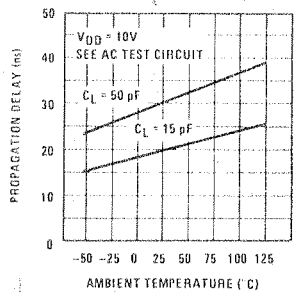
Power Dissipation vs Frequency



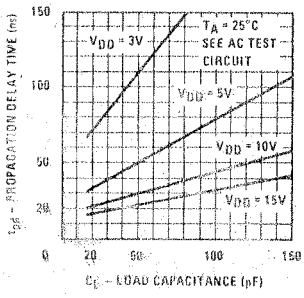
Propagation Delay vs Ambient Temperature



Propagation Delay vs Ambient Temperature



Propagation Delay Time vs Load Capacitance



5

National Semiconductor

CD4071BM/CD4071BC Quad 2-Input OR Buffered B Series Gate
CD4081BM/CD4081BC Quad 2-Input AND Buffered B Series Gate

General Description

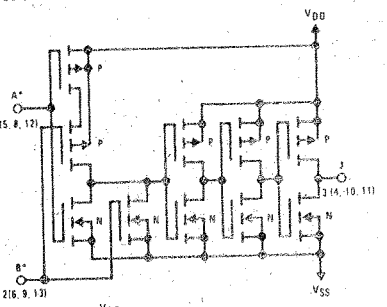
These quad gates are monolithic complementary MOS (CMOS) integrated circuits consructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

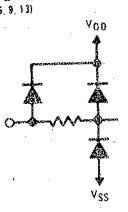
All inputs protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 5V–10–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1μA at 15V over full temperature range

Schematic and Connection Diagrams



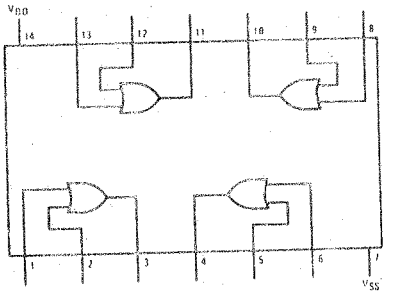


1/4 of device shown

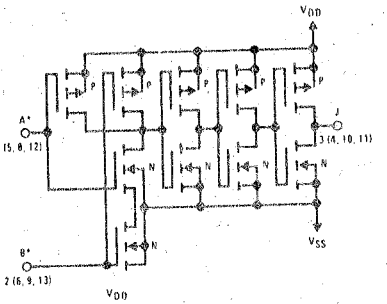
J = A + B
Logical "1" = High
Logical "0" = Low

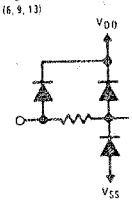
*All inputs protected by standard CMOS protection circuit

CD4071B
Dual-In-Line and Flat Package



TOP VIEW



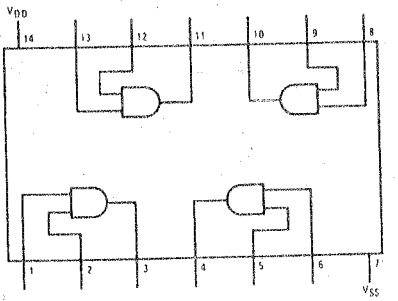


1/4 of device shown

J = A · B
Logical "1" = High
Logical "0" = Low

*All inputs protected by standard CMOS protection circuit.

CD4081B
Dual-In-Line and Flat Package



TOP VIEW

Absolute Maxim

(Notes 1 and 2)

Voltage at Any Pin
Package Dissipation
V_{DD} Range
Storage Temperature
Lead Temperature (Soldering,

DC Electrical Cha

	PARAMETER
I_{DD}	Quiescent Device Curre
V_{OL}	Low Level Output Volt
V_{OH}	High Level Output Volt
V_{IL}	Low Level Input Voltag
V_{IH}	High Level Input Voltag
I_{OL}	Low Level Output Curr
I_{OH}	High Level Output Curr
I_{IN}	Input Current

Note 1: "Absolute Maximum R
Temperature Range" they are n
provides conditions for actual dev
Note 2: All voltages measured wi

Absolute Maximum Ratings

(Notes 1 and 2)

Voltage at Any Pin	−0.5V to V_{DD} + 0.5V
Package Dissipation	500 mW
V_{DD} Range	−0.5 V_{DC} to +18 V_{DC}
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

Operating V_{DD} Range	3 V_{DC} to 15 V_{DC}
Operating Temperature Range	
CD4071BM, CD4081BM	−55°C to +125°C
CD4071BC, CD4081BC	−40°C to +85°C

DC Electrical Characteristics — CD4071BM/CD4081BM (Note 2)

PARAMETER	CONDITIONS	−55°C MIN	−55°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+125°C MIN	+125°C MAX	UNITS
I_{DD} Quiescent Device Current	V_{DD} = 5V		0.25		0.004	0.25		7.5	μA
	V_{DD} = 10V		0.50		0.005	0.50		15	μA
	V_{DD} = 15V		1.0		0.006	1.0		30	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
	V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
	V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95		V
	V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
	V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V		1.5		2	1.5		1.5	V
	V_{DD} = 10V, V_O = 1.0V		3.0		4	3.0		3.0	V
	V_{DD} = 15V, V_O = 1.5V		4.0		6	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	3		3.5		V
	V_{DD} = 10V, V_O = 9.0V	7.0		7.0	6		7.0		V
	V_{DD} = 15V, V_O = 13.5V	11.0		11.0	9		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
	V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
	V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
	V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN} Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

DC Electrical Characteristics

CD4071BC/CD4081BC (Note 2)

PARAMETER		CONDITIONS	−40°C MIN	−40°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.004	1		7.5	μA
		V_{DD} = 10V		2		0.005	2		15	μA
		V_{DD} = 15V		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics

CD4071BC/CD4071BM

T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L=200KΩ Typical temperature coefficient is 0.3%/°C

PARAMETER		CONDITIONS	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High-to-Low Level	V_{DD} = 5V	100	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	V_{DD} = 5V	90	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{THL},t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	18		pF

AC Electri

T_A = 25°C, Inp

t_{PHL}	P
t_{PLH}	P
t_{THL},t_{TLH}	T
C_{IN}	A
C_{PD}	P

Typical Pe

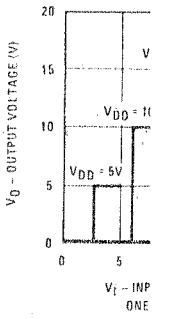


FIGURE 1.
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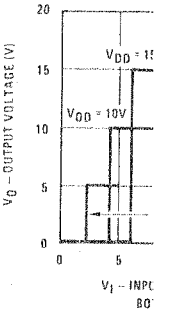


FIGURE 4.
Charact

°C		+85°C		UNITS
P	MAX	MIN	MAX	
04	1		7.5	μA
05	2		15	μA
06	4		30	μA
			0.05	V
	0.05		0.05	V
	0.05		0.05	V
		4.95		V
		9.95		V
		14.95		V
	1.5		1.5	V
	3.0		3.0	V
	4.0		4.0	V
		3.5		V
		7.0		V
		11.0		V
38		0.36		mA
25		0.9		mA
3		2.4		mA
38		−0.36		mA
25		−0.9		mA
3		−2.4		mA
−5	−0.30		−1.0	μA
−5	0.30		1.0	μA

0.3%/°C

	MAX	UNITS
	250	ns
	100	ns
	70	ns
	250	ns
	100	ns
	70	ns
	200	ns
	100	ns
	80	ns
	7.5	pF
		pF

AC Electrical Characteristics CD4081BC/CD4081BM

T_A = 25°C, Input t_r; t_f = 20 ns, C_L = 50 pF, R_L = 200K Typical temperature coefficient is 0.3%/°C

PARAMETER		CONDITIONS	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High-to-Low Level	V_{DD} = 5V	100	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{THL},t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	18		pF

Typical Performance Characteristics

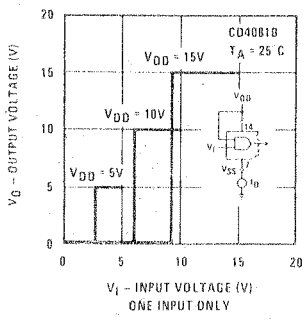


FIGURE 1. Typical Transfer Characteristics

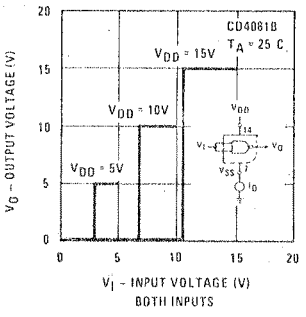


FIGURE 2. Typical Transfer Characteristics

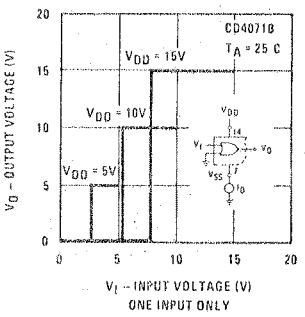


FIGURE 3. Typical Transfer Characteristics

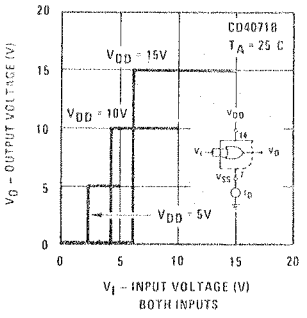


FIGURE 4. Typical Transfer Characteristics

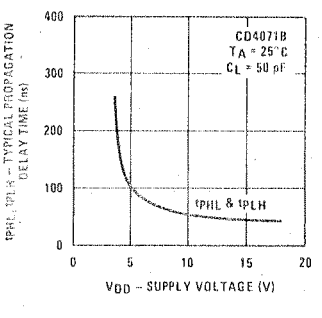


FIGURE 5

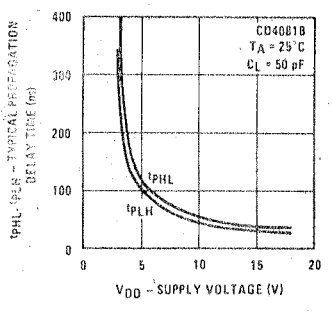


FIGURE 6

Typical Performance Characteristics (Cont'd.)

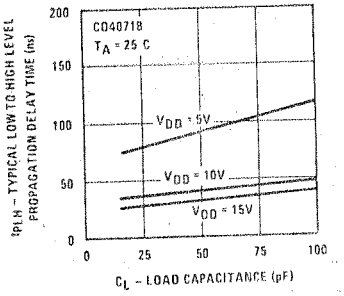


FIGURE 7

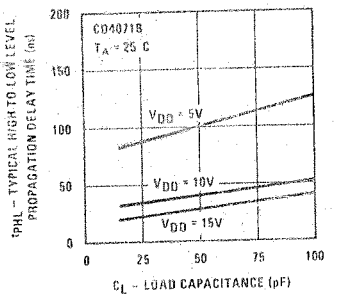


FIGURE 8

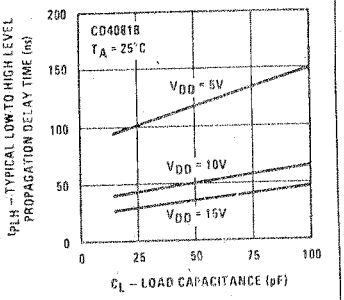


FIGURE 9

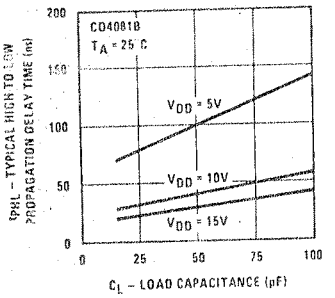


FIGURE 10

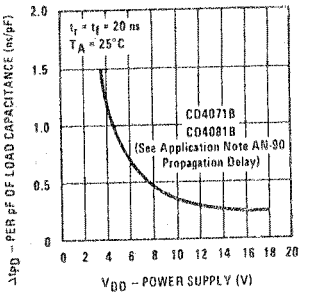


FIGURE 11

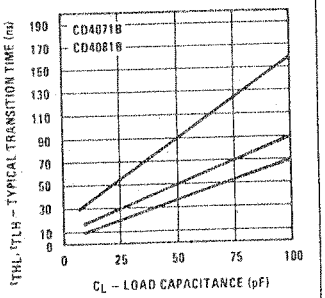


FIGURE 12

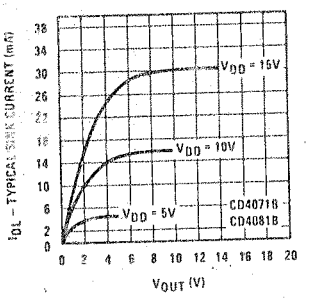


FIGURE 13

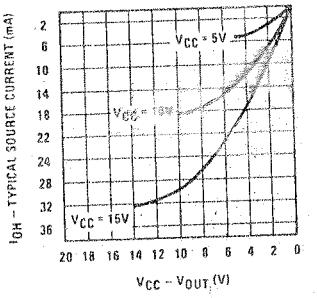


FIGURE 14

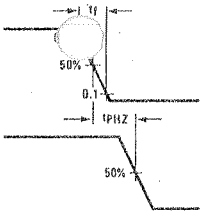
Nat
Sem

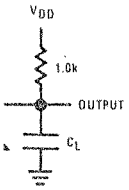
CD4072B
CD4082B

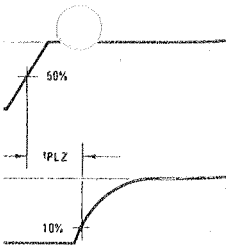
General Des

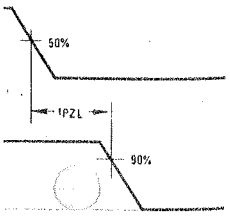
These dual gates
(CMOS) integrate
P-channel enhanc
equal source and
to standard B serie
buffered outputs w
by providing very
against static disc

Connection









National Semiconductor

CD4510BM/CD4510BC BCD Up/Down Counter
CD4516BM/CD4516BC Binary Up/Down Counter

General Description

The CD4510BM/CD4510BC and CD4516BM/CD4516BC are monolithic CMOS up/down counters which count in BCD and binary, respectively.

The counters count up when the up/down input is at logical "1" and vice versa. A logical "1" preset enable signal allows information at the parallel inputs to preset the counters to any state synchronously with the clock. The counters are advanced one count at the positive-going edge ofthe clock if the carry in, preset enable, and reset inputs are at logical "0". Advancement is inhibited when any of these three inputs are at logical "1". The carry out signal is normally at logical "1" state and goes to logical "0" when the counter reaches its maximum count in the "up" mode or its minimum count in the "down" mode, provided the carry input is at logical "0" state. The counters are cleared asynchronously by applying a logical "1" voltage level at the reset input.

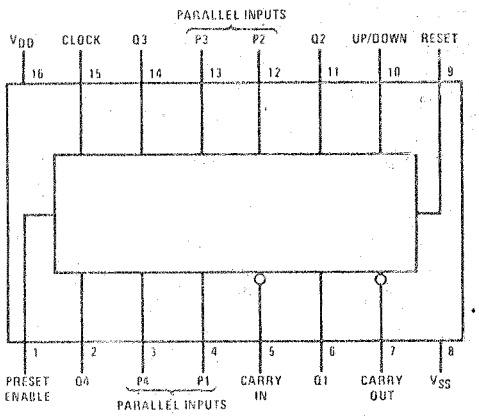
All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Parallel load "jam" inputs
- Low quiescent power dissipation — 0.25 μW/package (typ.) @ V_{CC} = 5.0 V
- Motorola MC14510, MC14516 second source

Connection Diagram

Dual-In-Line and Flat Package



TOP VIEW

Truth Table

CLOCK	RESET	PRESET ENABLE	CARRY IN	UP/DOWN	OUTPUT FUNCTION
X	1	X	X	X	Reset to zero
X	0	1	X	X	Set to P1, P2, P3, P4
↗	0	0	0	1	Count up
↗	0	0	0	0	Count down
↘	0	0	X	X	No change
X	0	0	1	X	No change

↗ = positive transition
↘ = negative transition
X = don't care

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} +0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditio

(Note 2)

V_{DD} dc Supply Voltage	3V to
V_{IN} Input Voltage	0 to
T_A Operating Temperature Range	−55°C to +1
CD4510BM, CD4516BM	−40°C to +
CD4510BC, CD4516BC	

DC Electrical Characteristics CD4510BM/CD4516BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UN
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.05	5		150	
		V_{DD} = 10V		10		0.1	10		300	
		V_{DD} = 15V		20		0.15	20		600	
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	
		V_{DD} = 10V		0.05		0	0.05		0.05	
		V_{DD} = 15V		0.05		0	0.05		0.05	
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		
		V_{DD} = 10V	9.95		9.95	10		9.95		
		V_{DD} = 15V	14.95		14.95	15		14.95		
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		
I_{OL}	Low Level Output Current	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.8		0.36		
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.0		0.9		
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	7.8		2.4		
I_{OH}	High Level Output Current	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.8		−0.36		
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.0		−0.9		
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−7.8		−2.4		
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	

DC Electrical Characteristics CD4510BC/CD4516BC (Note 2)

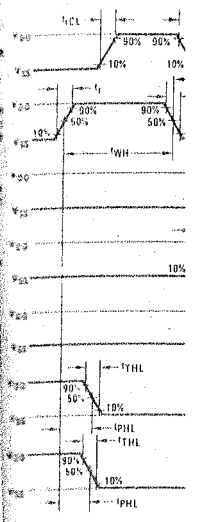
PARAMETER		CONDITIONS	−40°C		25°C			85°C	
			MIN	MAX	MIN	TYP	MAX	MIN	MAX
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.05	20		150
		V_{DD} = 10V		40		0.1	40		300
		V_{DD} = 15V		80		0.15	80		600
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\| < 1\ \mu A$							
		V_{DD} = 5V		0.05		0	0.05		0.05
		V_{DD} = 10V		0.05		0	0.05		0.05
		V_{DD} = 15V		0.05		0	0.05		0.05
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\| < 1\ \mu A$							
		V_{DD} = 5V	4.95		4.95	5		4.95	
		V_{DD} = 10V	9.95		9.95	10		9.95	
		V_{DD} = 15V	14.95		14.95	15		14.95	

DC Electrical C

PARAMETER	
V_{IL}	Low Level Input V
V_{IN}	High Level Input V
V_{OL}	Low Level Output
V_{OH}	High Level Output
	Input Current

1: "Absolute Maximun
the devices should be op
tions for actual device o
2: V_{SS} = 0V unless oth
3: Devices should not b

witching Time



d Operating Condition

ge 3V to 1
0 to V

ature Range
16BM −55°C to +12
16BC −40°C to +8

5°C		125°C		UNITS
TYP	MAX	MIN	MAX	
0.05	5		150	
0.1	10		300	
0.15	20		600	
)	0.05		0.05	
)	0.05		0.05	
)	0.05		0.05	
5		4.95		
10		9.95		
15		14.95		
2.25	1.5		1.5	
4.5	3.0		3.0	
6.75	4.0		4.0	
2.75		3.5		
5.5		7.0		
8.25		11.0		
1.8		0.36		
1.0		0.9		
1.8		2.4		
1.8		−0.36		
1.0		−0.9		
1.8		−2.4		
10^{-5}	−0.1		−1.0	
10^{-5}	0.1		1.0	

C		85°C		UNITS
P	MAX	MIN	MAX	
05	20		150	
1	40		300	
15	80		600	
	0.05		0.05	
			0.05	
	0.05		0.05	
		4.95		
		9.95		
		14.95		

DC Electrical Characteristics (Cont'd.) CD4510BC/CD4516BC (Note 2)

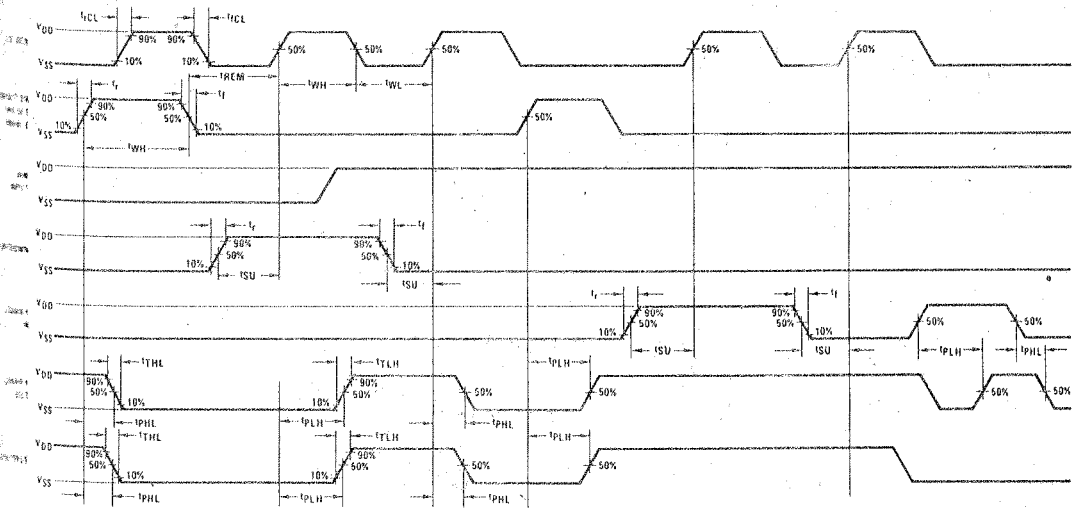
PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
Low Level Input Voltage	$\lvert I_O \rvert < 1\ \mu A$								
	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
	$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
	$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
High Level Input Voltage	$\lvert I_O \rvert < 1\ \mu A$								
	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
	$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
	$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
Low Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.8		0.36		mA
	$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.0		0.9		mA
	$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	7.8		2.4		mA
High Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
	$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.8		−0.36		mA
	$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.0		−0.9		mA
	$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−7.8		−2.4		mA
Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		1.0	μA
	$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: Devices should not be connected while power is "ON."

Switching Time Waveforms



AC Electrical Characteristics

CD4510BM/CD4510BC, CD4516BM/CD4516BC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$k, $t_{rCL} = t_{fCL} = t_r = t_f = 20$ ns, unless otherwise specified

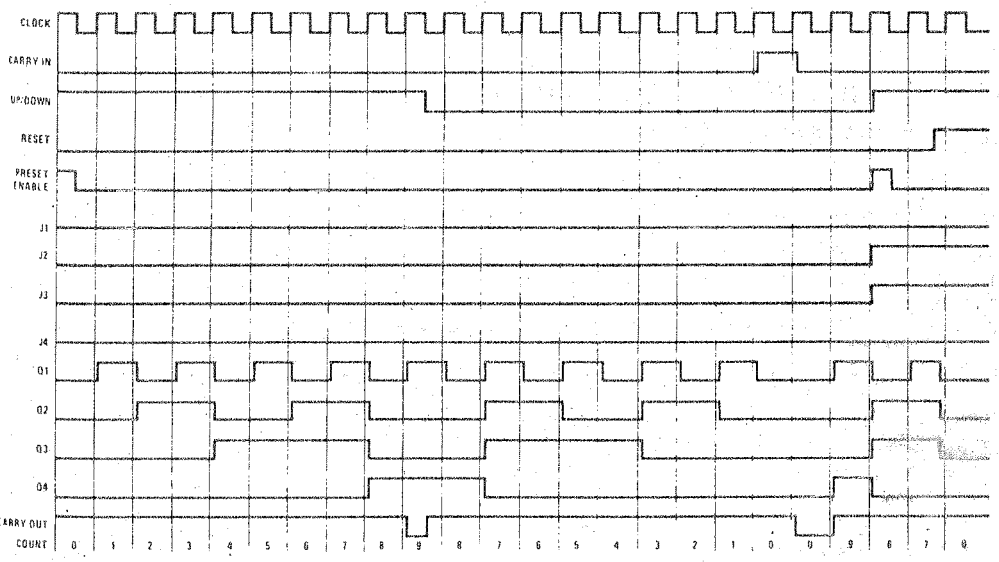
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKED OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Q Outputs	$V_{DD} = 5V$		220	500	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		80	180	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Carry Output	$V_{DD} = 5V$		315	630	ns
		$V_{DD} = 10V$		130	260	ns
		$V_{DD} = 15V$		100	200	ns
t_{THL}, t_{TLH}	Transition Time Q and Carry Outputs	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		160	315	ns
		$V_{DD} = 10V$		65	130	ns
		$V_{DD} = 15V$		50	100	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$	15			μs
		$V_{DD} = 10V$	15			μs
		$V_{DD} = 15V$	15			μs
t_{SU}	Minimum Carry In Set-Up Time	$V_{DD} = 5V$		100	220	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		35	70	ns
t_{SU}	Minimum Up/Down Set-Up Time	$V_{DD} = 5V$		200	420	ns
		$V_{DD} = 10V$		70	170	ns
		$V_{DD} = 15V$		60	150	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1.5	3.1		MHz
		$V_{DD} = 10V$	3.8	7.6		MHz
		$V_{DD} = 15V$	5.0	10.0		MHz
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 4)	Per Package,		65		pF
RESET/PRESET ENABLE OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Reset/ Preset Enable to Q Output	$V_{DD} = 5V$		285	570	ns
		$V_{DD} = 10V$		115	230	ns
		$V_{DD} = 15V$		95	195	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Reset/ Preset Enable to Carry Output	$V_{DD} = 5V$		420	860	ns
		$V_{DD} = 10V$		170	350	ns
		$V_{DD} = 15V$		140	290	ns
t_{WH}	Minimum Reset/Preset Enable Pulse Width	$V_{DD} = 5V$		90	200	ns
		$V_{DD} = 10V$		40	100	ns
		$V_{DD} = 15V$		35	80	ns
t_{REM}	Minimum Reset/Preset Enable Removal Time	$V_{DD} = 5V$		170	330	ns
		$V_{DD} = 10V$		70	140	ns
		$V_{DD} = 15V$		60	120	ns
CARRY INPUT OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Carry In to Carry Output	$V_{DD} = 5V$		260	500	ns
		$V_{DD} = 10V$		110	220	ns
		$V_{DD} = 15V$		90	180	ns

Note 4: Dynamic power dissipation (P_D) is given by: $P_D = (C_{PD} + C_L)V_{DD}^2 f + P_Q$; where C_L = load capacitance; f = frequency of
P_Q = Quiescent Power Dissipation. For further details, see application note AN-90, "54C/74C Family characteristics."

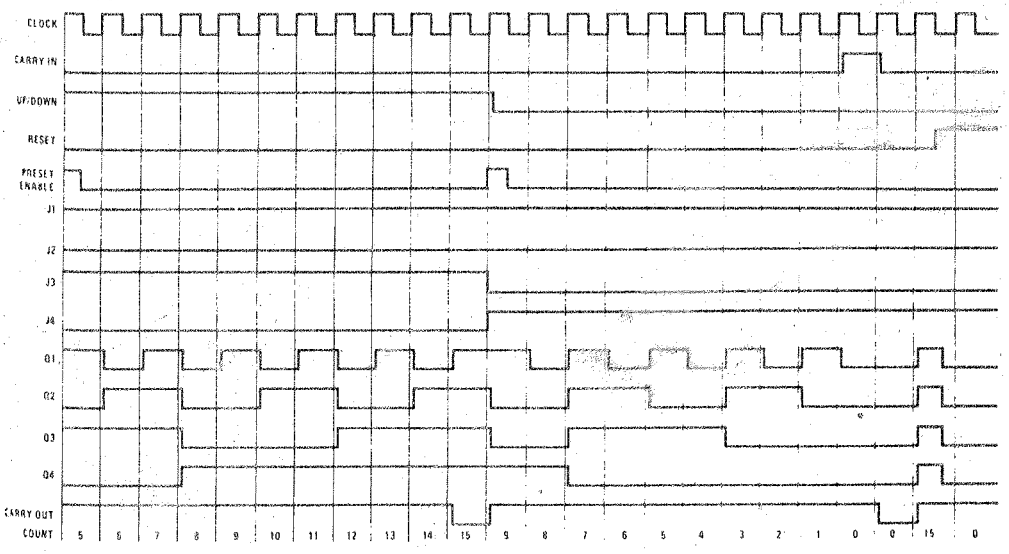
Cascading Pac

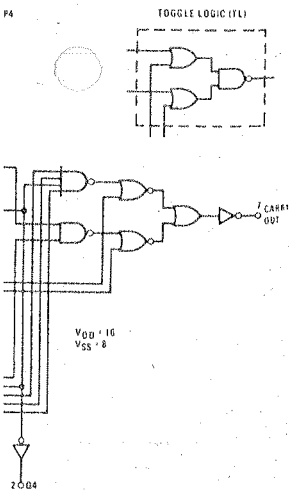
Logic Waveforms

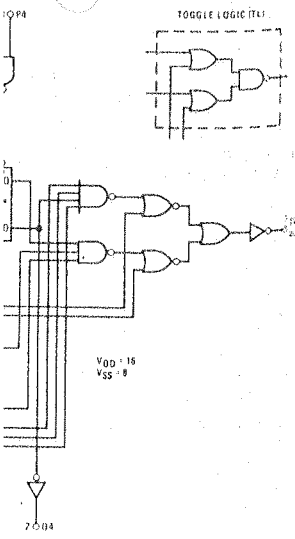
CD4510BM/CD4510BC



CD4516BM/CD4516BC







Am2716/Am9716

2048 x 8-Bit UV Erasable PROM

MILITARY, INDUSTRIAL AND COMMERCIAL

DISTINCTIVE CHARACTERISTICS

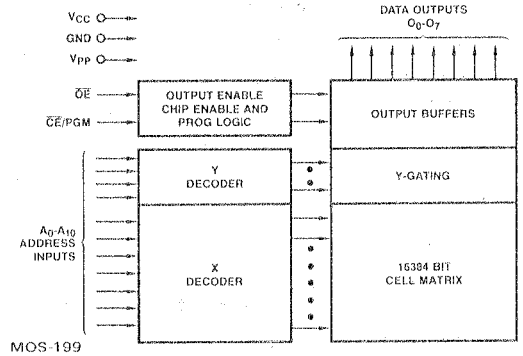
- 0.3% AQL guaranteed
- Direct replacement for Intel 2716
- Interchangeable with Am9218 – 16K ROM
- Single +5V power supply
- Fast access time – 450ns standard with 300ns, 350ns and 390ns options
- Low power dissipation
  - 525mW active
  - 132mW standby
- Fully static operation – no clocks
- Three-state outputs
- TTL compatible inputs/outputs
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

The Am2716/Am9716 is a 16384-bit ultraviolet erasable and programmable read-only memory. It is organized as 2048 words by 8 bits per word, operates from a single +5V supply, has a static standby mode and features fast single address location programming.

Because the Am2716/Am9716 operates from a single +5V supply, it is ideal for use in microprocessor systems. All programming signals are TTL levels, requiring a single pulse. For programming outside of the system, existing EPROM programmers may be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 100 seconds.

BLOCK DIAGRAM



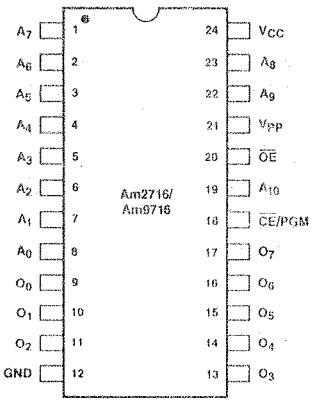
MOS-199

MODE SELECTION

Mode \ Pins	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

CONNECTION DIAGRAMS – Top Views

DIP

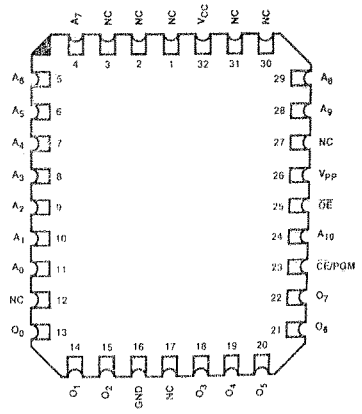


Note: Pin 1 is marked for orientation

A_0-A_{10}: Addresses
O_0-O_7: Outputs
$\overline{CE}$/PGM: Chip Enable/Program
$\overline{OE}$: Output Enable

MOS-200

Chip-Pak™ L-32-2



MOS-672

Chip-Pak is a trademark of Advanced Micro Devices, Inc.

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65 to +150°C
Ambient Temperature Under Bias	−65 to +135°C
Voltage on All Inputs/Outputs (except V_{PP}) with Respect to GND	+6V to −0.3V
Voltage on V_{PP} During Program with Respect to GND	+26.5V to −0.3V

DC AND AC READ OPERATIONS CONDITIONS (Notes 1, 2)

	Temperature Range	V_{CC}	V_{PP}
AM2716DC/AM2716-2DC	0 to +70°C	5V ± 5%	V_{PP} (Note 2) = V_{CC} For all device types
AM9716DC/AM2716-1DC	0 to +70°C	5V ± 10%	
AM2716DI/AM2716-1DI	−40 to +85°C	5V ± 5%	
AM2716DL/AM2716-1DL	−55 to +100°C	5V ± 10%	
AM2716DM	−55 to +125°C	5V ± 10%	

DC CHARACTERISTICS

Parameters	Description	Test Conditions	Min Values	Maximum Values			Units
			All Types	DL/DM	DI	DC	
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ (Max) and $V_{IN} = 0$		10	10	10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ (Max) and $V_{OUT} = 0$		10	10	10	μA
I_{PP1} (Note 2)	V_{PP} Current	$V_{PP} = V_{CC}$ (Max)		5	5	5	mA
I_{CC1} (Note 2)	V_{PP} Current (Standby)	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$		30	30	25	mA
I_{CC2} (Note 2)	V_{CC} Current (Active)	$\overline{OE} = \overline{CE} = V_{IL}$		115	110	100	mA
V_{IL}	Input Low Voltage		−0.1	0.8	0.8	0.8	Volts
V_{IH}	Input High Voltage		2.0	$V_{CC}+1$	$V_{CC}+1$	$V_{CC}+1$	Volts
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA @ V_{CC} (Min)		0.45	0.45	0.45	Volts
V_{OH}	Output High Voltage	I_{OH} = −400μA @ V_{CC} (Min)	2.4				Volts

AC CHARACTERISTICS

Parameters	Description	Test Conditions (Note 3)	Min Values	Maximum Values						Units
			All Types	9716 DC	2716-1 DC	2716-2 DC	2716 DC	2716-1 DI/DL	2716 DI/DL/DM	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		300	350	390	450	350	450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		300	350	390	450	350	450	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$		120	120	120	120	150	150	ns
t_{DF}	Output Enable High to Output Float	$\overline{CE} = V_{IL}$	0	100	100	100	100	130	130	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0							ns

CAPACITANCE (Note 4)

T_A = +25°C, f = 1MHz

Parameters	Description	Test Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Other Test Conditions: a) Output Load: 1 TTL gate and C_L = 100pF
b) Input Rise and Fall Times: ≤20ns
c) Input Pulse Levels: 0.8 to 2.2V
d) Timing Measurement Reference Level:
Inputs: 1V and 2V
Outputs: 0.8V and 2V
4. This parameter is only sampled and is not 100% tested.

ADDRESSES

$\overline{CE}$

$\overline{OE}$

OUTPUT

Notes:

−65 to +150°C
−65 to +135°C
+6V to −0.3V
+26.5V to −0.3V

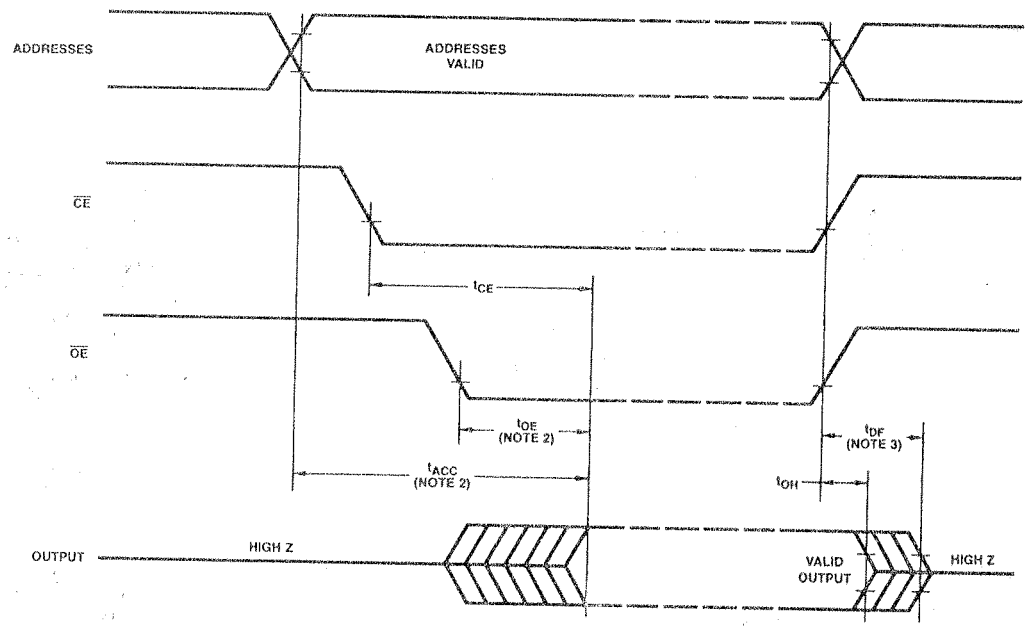
lues DC	Units
10	μA
10	μA
5	mA
25	mA
100	mA
0.8	Volts
V_{CC} +1	Volts
0.45	Volts
	Volts

716-1 DI/DL	16 DI/DL/DM	Units
350	450	ns
350	450	ns
150	150	ns
130	130	ns
		ns

Units
pF
pF

I_{CC} and I_{PP1}.

AC WAVEFORMS (Note 1)



MOS-201

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

ORDERING INFORMATION

Ambient Temperature Specification	Order Number	t_{ACC} (ns)	t_{CE} (ns)	t_{OE} (ns)
0°C ≤ T_A ≤ 70°C	AM9716DC	300	300	120
	AM9716LC			
	AM2716-1DC	350	350	120
	AM2716-1LC			
	AM2716-2DC	390	390	120
	AM2716-2LC			
	AM2716DC	450	450	120
	AM2716LC			
−40°C ≤ T_A ≤ +85°C	AM2716-1DI	350	350	150
	AM2716-1LI			
	AM2716DI	450	450	150
	AM2716LI			
−55°C ≤ T_A ≤ +100°C	AM2716-1DL	350	350	150
	AM2716-1LL			
	AM2716DL	450	450	150
	AM2716LL			
−55°C ≤ T_A ≤ +125°C	AM2716DM	450	450	150
	AM2716LM			

PROGRAM OPERATION

DC PROGRAMMING CHARACTERISTICS

T_A = +25°C ±5°C, V_{CC} (Note 1) = 5V ±5%, V_{PP} (Notes 1, 2) = 25V ±1V

Parameters	Description	Test Conditions	Min	Max	Units
I_{LI}	Input Current	V_{IN} = 5.25/0.45V		10	μA
I_{PP1}	V_{PP} Supply Current	$\overline{CE}$/PGM = V_{IL}		5	mA
I_{PP2}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}$/PGM = V_{IH}		30	mA
I_{CC}	V_{CC} Supply Current			100	mA
V_{IL}	Input Low Level		−0.1	0.8	Volts
V_{IH}	Input High Level		2.0	V_{CC}+1	Volts

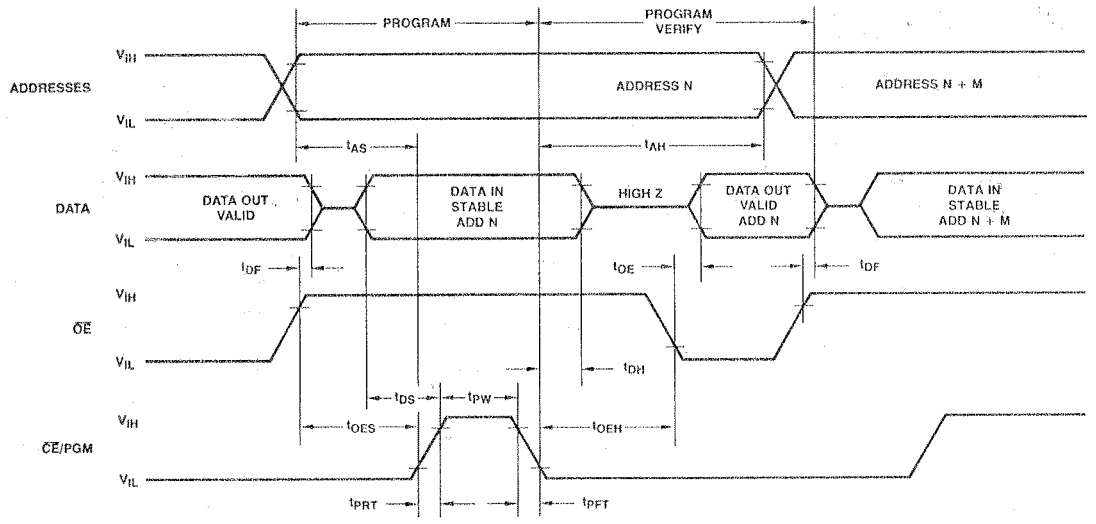
AC PROGRAMMING CHARACTERISTICS

T_A = +25°C ±5°C, V_{CC} (Note 1) = 5V ±5%, V_{PP} (Notes 1, 2) = 25V ±1V

Parameters	Description	Test Conditions	Min	Max	Units
t_{AS}	Address Set-up Time	Input t_R and t_F (10% to 90%) = 20ns Input Signal Levels = 0.8 to 2.2V Input Timing Reference Level = 1V and 2V Output Timing Reference Level = 0.8V and 2V	2		μs
t_{OES}	Output Enable Set-up Time		2		μs
t_{DS}	Data Set-up Time		2		μs
t_{AH}	Address Hold Time		2		μs
t_{OEH}	Output Enable Hold Time		2		μs
t_{DH}	Data Hold Time		2		μs
t_{DF}	Output Disable to Output Float Delay ($\overline{CE}$/PGM = V_{IL})		0	120	ns
t_{OE}	Output Enable to Output Delay ($\overline{CE}$/PGM = V_{IL})		–	120	ns
t_{PW}	Program Pulse Width		45	55	ms
t_{PRT}	Program Pulse Rise Time		5	–	ns
t_{PFT}	Program Pulse Fall Time		5	–	ns

Notes: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} must not be greater than 26 volts including overshoot. Permanent device damage may occur if the device is taken out of or put into the socket when V_{PP} = 25 volts is applied. Also, during $\overline{OE}$ = $\overline{CE}$/PGM = V_{IH}, V_{PP} must not be switched from 5 volts to 25 volts or vice versa.

PROGRAMMING WAVEFORMS



MOS-202

ERASING THE Am2716/

In order to clear all locatic necessary to expose the source. A dosage of 15 W erase an Am2716/Am971 exposure to an ultraviolet (Å)] with intensity of 120 Am2716/Am9716 should b all filters should be remo erasure.

It is important to note that vices, will erase with light than 4000 Angstroms. A longer than with UV source to florescent light and sunl Am9716, and exposure to maximum system reliabilit package windows should substance.

PROGRAMMING THE A

Upon delivery, or after eac 16384 bits in the "1," or Am2716/Am4716 through

The programming mode is V_{PP} pin and when $\overline{OE}$ is at applied to the proper addr the respective data outpu standard TTL levels. Wher a 50msec, TTL high level p accomplish the programm

The procedure can be dor domly, or automatically via is that one 50msec progra be programmed. It is nece exceed 55msec. Therefor input is prohibited when p

READ MODE

The Am2716/Am9716 has must be logically satisfied Chip Enable ($\overline{CE}$) is the p device selection. Output

Max	Units
10	μA
5	mA
30	mA
100	mA
0.8	Volts
$V_{CC}+1$	Volts

Min	Max	Units
2		μs
2		μs
2		μs
2		μs
2		μs
2		μs
0	120	ns
–	120	ns
45	55	ms
5	–	ns
5	–	ns

ɔn out of or put into the socket
25 volt ice versa.

SS N + M

DATA IN
STABLE
ADD N + M

MOS 202

ERASING THE Am2716/Am9716

In order to clear all locations of their programmed contents, it is necessary to expose the Am2716/Am9716 to an ultraviolet light source. A dosage of 15 Wseconds/cm^2 is required to completely erase an Am2716/Am9716. This dosage can be obtained by exposure to an ultraviolet lamp [wavelength of 2537 Angstroms (Å)] with intensity of 12000μW/cm^2 for 15 to 20 minutes. The Am2716/Am9716 should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am2716/Am9716, and similar devices, will erase with light sources having wavelengths shorter than 4000 Angstroms. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to florescent light and sunlight will eventually erase the Am2716/Am9716, and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

PROGRAMMING THE Am2716/Am9716

Upon delivery, or after each erasure the Am2716/Am9716 has all 16384 bits in the "1," or high state. "0s" are loaded into the Am2716/Am4716 through the procedure of programming.

The programming mode is entered when +25V is applied to the V_{PP} pin and when $\overline{OE}$ is at V_{IH}. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data output pins. The voltage levels should be standard TTL levels. When both the address and data are stable, a 50msec, TTL high level pulse is applied to the $\overline{CE}$/PGM input to accomplish the programming.

The procedure can be done manually, address by address, randomly, or automatically via the proper circuitry. All that is required is that one 50msec program pulse be applied at each address to be programmed. It is necessary that this program pulse width not exceed 55msec. Therefore, applying a DC level to the $\overline{CE}$/PGM input is prohibited when programming.

READ MODE

The Am2716/Am9716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}) for all devices. Data is available at the outputs 120ns or 150ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The Am2716/Am9716 has a standby mode which reduces the active power dissipation by 75%, from 525mW to 132mW (values for 0 to +70°C). The Am2716/Am9716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

To accommodate multiple memory connections, a 2-line control function is provided to allow for:

1. Low memory power dissipation
2. Assurance that output bus contention will not occur.

It is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAM INHIBIT

Programming of multiple Am2716/Am9716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel Am2716/Am9716s may be common. A TTL level program pulse applied to an Am2716/Am9716's $\overline{CE}$/PGM input with V_{PP} at 25V will program that Am2716/Am9716. A low level $\overline{CE}$/PGM input inhibits the other Am2716/Am9716 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at V_{CC}.